KnowMade

GaN Newsletter

December 2024

Powered by Knowmade every month, the **GaN newsletter** presents a selection of the latest **scientific publications**, **patent applications** and **news** related to **III-Nitride semiconductors** (GaN, AlN, InN and alloys) for **optoelectronic** and **electronic** applications (power, RF, LED, laser, photonics, etc.).

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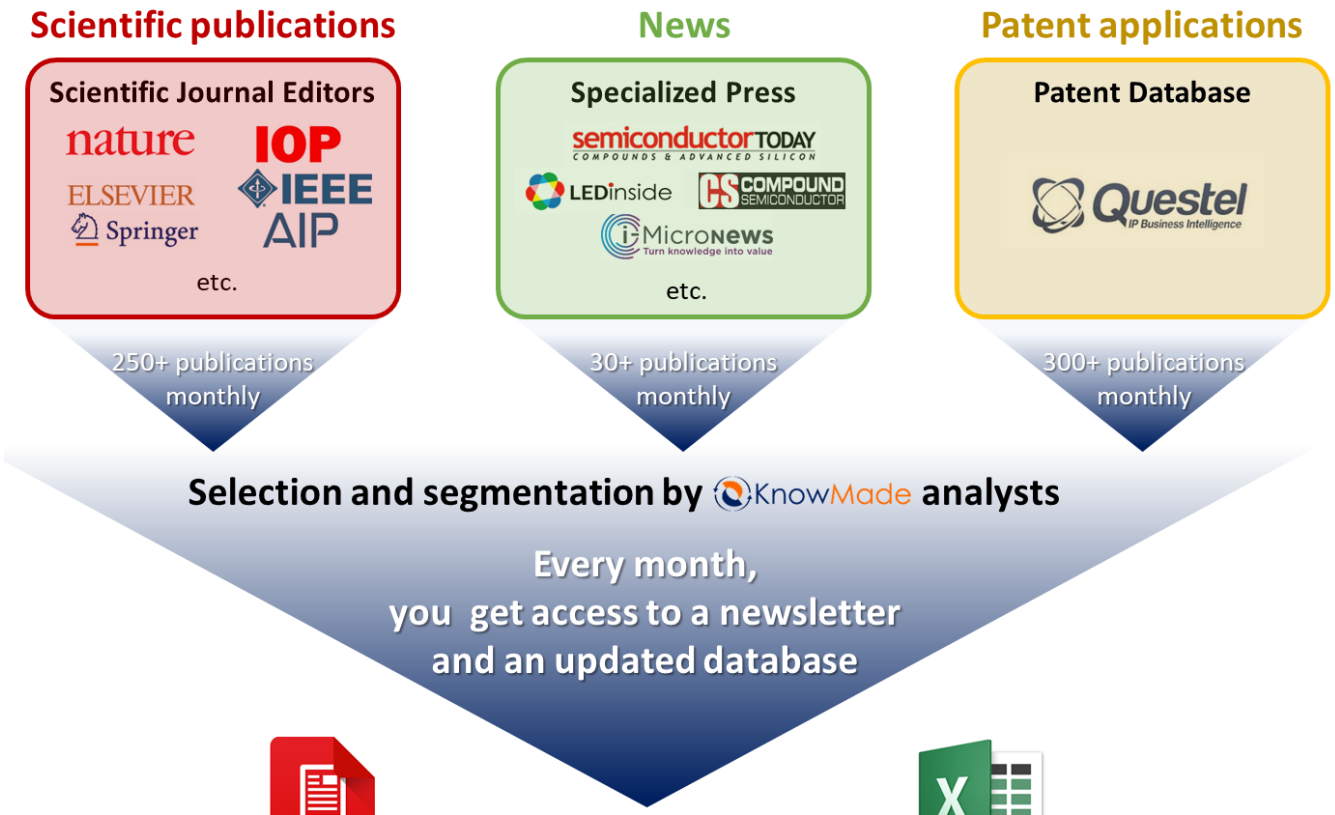
Table of contents

Clickable links to sections

METHODOLOGY & CONTENT



GaN newsletter

New scientific publications
- Optoelectronics
- Electronics

News
- Optoelectronics
- Electronics
- Others

New patent applications
- Statistical overview
- Notable patent applications

The newsletter focuses on the new publications of the month in optoelectronics (LED, µ-LED, laser, photonics, etc.) and electronics (power, RF and other advanced electronic devices).

GaN database

All scientific publications
- Optoelectronics
- Electronics
- MEMS & Sensors
- PV & Energy harvesting
- Nano-objects
- Non-polar & Semi-polar
- Fundamental & Materials

All news

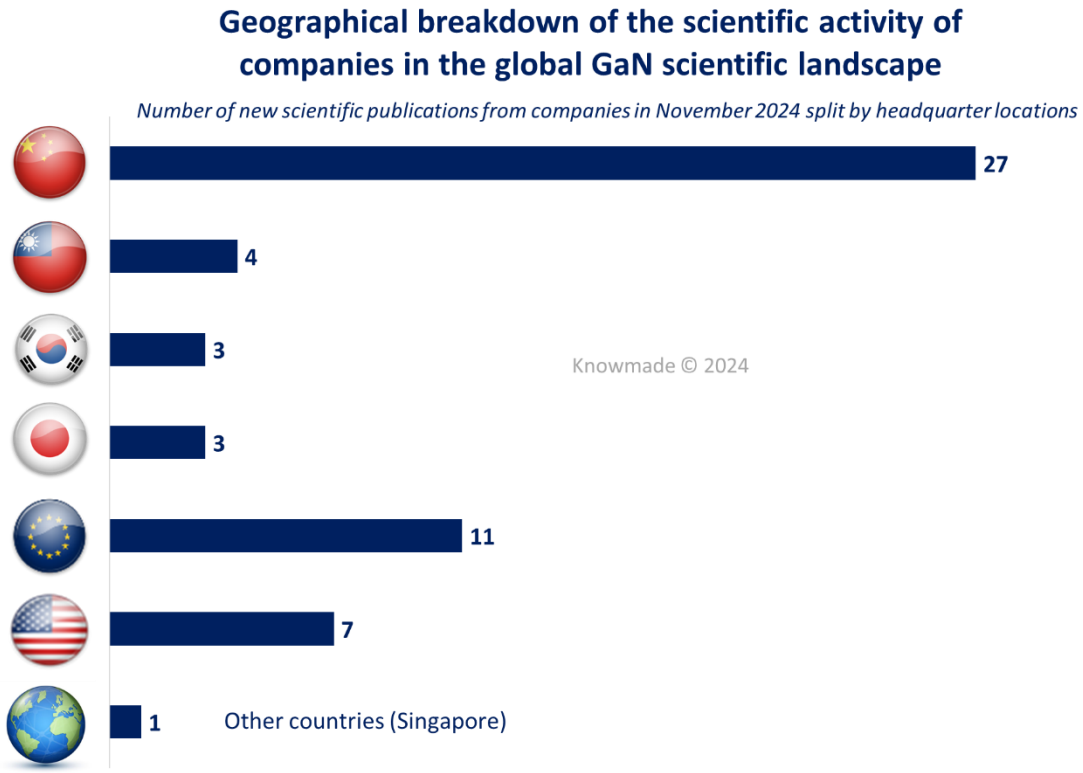
All patent applications
(Premium version only)

The database is updated every month with new publications related to GaN with a segmentation of scientific publications in 7 categories.

SCIENTIFIC PUBLICATIONS

More than **230 new scientific publications** related to GaN technology were selected last month, of which **70+ publications related to GaN optoelectronics** (LED, laser, photonics, photodetectors) and **100+ publications related to GaN electronics** (Power, RF and advanced electronics):

Furthermore, **various companies** have been involved in the publications of at least **55 scientific papers** related to GaN technology last month:



Strain-concentration for fast, compact photonic modulation and non-volatile memory

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Optica
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A critical figure of merit (FoM) for electro-optic (EO) modulators is the transmission change per voltage, dT/dV. Conventional approaches in wave-guided modulators maximize dT/dV via a high EO coefficient or longer light-material interaction lengths but are ultimately limited by material losses and nonlinearities. Optical and RF resonances improve dT/dV at the cost of spectral non-uniformity, especially for high-Q optical cavity resonances. Here, we introduce an EO modulator based on piezo-strain-concentration of a photonic crystal cavity to address both trade-offs: (i) it eliminates the trade-off between dT/dV and waveguide loss—i.e., enhancement of the resonance tuning efficiency dvc/dV for the fixed EO coefficient, waveguide length, and cavity Q—and (ii) at high DC strains it exhibits a non-volatile (NV) cavity tuning Δvc,NV for passive memory and programming of multiple devices into resonance despite fabrication variations. The device is fabricated on a scalable silicon nitride-on-aluminum nitride platform. We measure dvc/dV=177±1MHz/V, corresponding to Δvc=40±0.32GHz for a voltage spanning ±120V with an energy consumption of $\delta U/\Delta vc$=0.17nW/GHz. The modulation bandwidth is flat up to ωBW,3dB/2π=3.2±0.07MHz for broadband DC-AC and 142±17MHz for resonant operation near a 2.8 GHz mechanical resonance. Optical extinction up to 25 dB is obtained via Fano-type interference. Strain-induced beam-buckling modes are programmable under a "read-write" protocol with a continuous, repeatable tuning range of 5±0.25GHz, allowing for storage and retrieval, which we quantify with mutual information of 2.4 bits and a maximum non-volatile excursion of 8 GHz. Using a full piezo-optical finite-element-model (FEM) we identify key design principles for optimizing strain-based modulators and chart a path towards achieving performance comparable to lithium niobate-based modulators and the study of high strain physics on-chip.

GaN Photonic Crystals: Spectral Dynamics in UV, X-Ray, and Alpha Radiation

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Advanced Photonics Research
https://doi.org/10.1002/adpr.202400075

In this work, a comparative analysis of gallium nitride (GaN) thin films is conducted, both with and without photonic crystal (PhC) structures, focusing on their scintillation and photoluminescence properties. GaN's suitability for diverse optoelectronic and radiation detection applications is analyzed, and this study examines how PhC implementation can enhance these properties. Methodologically, the emission spectra is analyzed from 5.9 keV X-ray sources, decay curves, pulse height spectra in response to 241Am 5.5 MeV alpha-rays, and photoluminescence spectra induced by UV excitation. The findings demonstrate a substantial increase in quantum efficiency for PhC GaN, nearly tripling the light yield that of conventional plain GaN thin films under the UV excitation. The enhancement is predominantly attributed to the PhC GaN's proficiency in guiding light at 550 nm, a feature indicative of its spectral filtering capabilities, as detailed in the study. Furthermore, side-band scintillations, stemming from inherent materials like Chromium that generate scintillations at diverse wavelengths, are effectively mitigated. A key finding of this study is the effective detection of light not only at

the rear but also along the lateral sides of the films, offering new possibilities for radiation detector design and architecture.

Optical and Visual Performance of PWM Controlled InGaN and InGaAlP LEDs for Automotive Lighting Applications

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IEEE Photonics Journal
https://doi.org/10.1109/JPHOT.2024.3489725

This research investigates the light quality and thermal management of InGaN and InGaAlP Light Emitting Diodes (LEDs) under various light regulation methods. We compare Continuous Wave (CW) and Pulse-Width Modulation (PWM) modes, examining their impacts on luminous flux, temperature, total color shift, and angular color shift. Our findings reveal that the CW mode offers higher luminous flux and reduced temperatures, while the PWM mode ensures enhanced color stability across different currents and viewing angles, especially for white LEDs; however, this stability does not extend to other LED types. From both optical and visual performance perspectives, the study emphasizes optimizing the driving current to meet regulatory requirements and ensure consistent color perception. These insights are crucial for automotive lighting design, contributing to improved regulatory compliance and aesthetic quality.

Short range optical communication with GaN-on-Si microLED and microPD matrices

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Journal of Society for Information Display
https://doi.org/10.1002/jsid.2012

(In)GaN microLEDs have reached a high degree of maturity due to their development in the lighting industry. Their robustness and high efficiency make them ideal candidates for high-brightness, high-resolution micro-displays. Beyond display applications, microLEDs are being explored for non-display uses, including wireless Visible Light Communication (VLC) and parallel communication via multicore fiber. This study investigates short-range chip-to-chip optical communication using InGaN/GaN microLEDs and micro Photodiodes (microPDs). Leveraging processes developed for micro-displays, we address the challenges of integrating GaN microLEDs and microPDs on ASICs. We outline the main figures of merit, including expected energy efficiency, optical coupling to multicore fibers or waveguides, and the spectral efficiency of InGaN/GaN microPDs correlated with TCAD simulation and experimental transmission results. Our study highlights the potential of GaN microLEDs and microPDs for massively parallel, energy-efficient data transmission, paving the way for innovative short-range and energy-efficient optical communication solutions.

Design of electron blocking layer and its influence on the radial hole transport in GaN-based vertical cavity surface emitting laser diodes

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Optics Express
https://doi.org/10.1364/OE.541259

The radial transport behavior of holes and the lateral insulation confinement of carriers in GaN-based vertical cavity surface emitting lasers (VCSELs) are investigated by modifying the design of the electron blocking layer (EBL). The calculation results indicate that the increased efficiency of hole injection into the current aperture region is the primary factor contributing to the improved laser output power observed with higher EBL doping concentrations. The energy band diagrams show that an increased EBL doping concentration can reduce the band bending, thereby affecting hole transport pathways. A new

composite EBL structure is proposed, which can further decrease the band bending in the EBL region, resulting in an enhanced hole transport capability toward the center of the current aperture. Therefore, the radiative recombination rate in quantum wells is improved by enhancing the coupling between the carriers and the central optical field. This research offers insight into the structural design of high-performance GaN-based VCSELs.

Size-dependent competitive effect between surface recombination and self-heat on efficiency droop for 250 nm AlGaN-based DUV LEDs

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Optics Letters
https://doi.org/10.1364/OL.539333

In this work, electrical and optical performances for 250 nm AlGaN-based flip-chip deep ultraviolet light emitting diodes (DUV LEDs) with different chip sizes are studied. Reduced chip size helps increase the light extraction efficiency (LEE) with the cost of increased surface nonradiative recombination. Nevertheless, a thin p-Al0.67-0Ga0.33-1N layer of 10 nm can manage current distribution while suppressing surface recombination and reducing light absorption simultaneously, which results in the increased optical power density. Thanks to the better current management and reduced optical self-absorption effect, the reduced Joule heating effect suppresses the thermal droop of the optical power density for a small DUV LED chip. We also find that the p-Al0.67-0Ga0.33-1N layer thickness shows very significant impact on device resistance especially for the small DUV LED chip, such that the device resistance has a remarkable increase when the p-Al0.67-0Ga0.33-1N layer is thickened to 100 nm.

Ultraviolet to mid-infrared optical properties of sputtered Al(Sc)N-on-SiO2 thin films and experimental demonstration of AlN integrated photonic devices in the telecom C-band

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Optics Express
https://doi.org/10.1364/OE.540975

Thin film aluminum nitride (AlN) stands out as a promising material for integrated photonics due to its wide bandgap of 6.1 eV, facilitating efficient operation across diverse spectral ranges. Its inherent electro-optic and nonlinear optical properties make it exceptionally well suited for active photonic components. Compatibility with CMOS technology further strengthens its appeal. Doping AlN with scandium (Sc) in non-centrosymmetric configurations significantly enhances its nonlinear and piezoelectric characteristics. This study explores Al(Sc)N thin films on silicon dioxide (SiO2), investigating optical properties in a broad wavelength range from 0.19 µm to 25 µm. Comprehensive material analysis of sputtered Al(Sc)N films and fabrication techniques for AlN integrated photonic devices demonstrated here highlight AlScN's potential in integrated photonic applications.

Improved Wavelength Stability of InGaN Based Red LEDs Grown on Graphene/SiC Substrates

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IEEE Electron Device Letters
https://doi.org/10.1109/LED.2024.3496940

The application of InGaN based red LEDs in Micro LED display has been severely limited due to their low luminous efficiency and poor wavelength stability. In this work, we demonstrate InGaN based red LEDs with improved wavelength stability on SiC substrates. The key of our method is to introduce a graphene intermediate layer between the epitaxial LED structure and SiC substrate. Another important process is to modulate the growth behavior and stress state of the

GaN film and LED structure on graphene. This is achieved by optimizing the nitrogen-plasma pre-treatment time of graphene. As a consequence, InGaN based red LEDs with small wavelength shift with the change of driving current are obtained. The wavelength shift is 8 nm as the forward driving current density increase from 1 to 10 A/cm 2 , which is significantly lower than the 25 nm of the reference red LEDs directly grown on SiC substrates. In addition, we analyse the mechanism responds to the improvements of wavelength stability for the red LEDs grown on graphene/SiC. This work provides a feasible approach for enhancing the wavelength stability of InGaN based red LEDs.

Large modulation bandwidth GaN-based micro-LED arrays on Si Substrates with graded In composition barriers

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IEEE Electron Device Letters
https://doi.org/10.1109/LED.2024.3495654

With the increasing wireless capacity demand for in sixth-generation (6G) networks exacerbating the issue of spectrum scarcity, high-speed visible light communication (VLC) based on GaN-based light-emitting diodes (LEDs) has emerged as a crucial supplementary solution. However, the lack of LED performance severely limits the development of VLC. Herein, the blue micro-LED array with the gradient of In component in the InxGa1-xN quantum barrier (QB) was demonstrated. Among them, the micro-LED array of two QBs with linearly increasing In component along [0001] direction serves to effectively suppress the polarization electric field, thereby increasing the radiative recombination efficiency and carrier concentration. At the current density of 2000 A/cm2, the light output power (LOP) is 28.9 mW, and the -3 dB bandwidth reaches 580 MHz, approximately 34% higher than that of the GaN barrier. This work presents a novel and simple strategy for realizing a high modulation bandwidth micro-LED array.

Design Principles and Performance Limitation of InGaN Nanowire Photonic Crystal Micro-LEDs

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IEEE Photonics Journal
https://doi.org/10.1109/JPHOT.2024.3511344

While micro-LEDs are crucial for ultrahigh resolution micro-displays, the efficiency of currently reported micro-LEDs degrades dramatically with decreasing size. Recently, the bottom-up nanowire approach has shown promise to break the efficiency bottleneck of this size effect. In this article, we investigated the design of nanowire photonic crystal structure for micro-LED applications and revealed its correlation with the Purcell effect. Key performance characteristics including efficiency, emission directionality, and spectral linewidth are thoroughly studied. For an LED structure with low internal quantum efficiency (IQE) of 10% due to high non-radiative recombination, an enhancement of ~30% is found viable by using a properly designed photonic crystal. High emission directionality and a narrow spectral linewidth (~ 5 nm) can be obtained with 60% of the light being emitted within a 20° acceptance angle.

Improved hole injection for AlGaN-based DUV LEDs with graded-composition multiple quantum barrier insertion layers

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Applied Optics
https://doi.org/10.1364/AO.541090

The primary impediments to achieving high external quantum efficiency (EQE) and light output power (LOP) in AlGaN-based deep-ultraviolet light-emitting diodes (DUV LEDs) are inadequate hole injection efficiency and pronounced electron leakage. The significant polarization-induced positive charges, originating from

the discontinuity in the Al composition between the last quantum barrier (LQB) and electron-blocking layer (EBL), attract electrons, consume holes, and reflect holes back into the p-type region, leading to severe electron leakage and low hole injection efficiency. In this paper, we introduce a graded-composition multiple quantum barrier (GQB) structure at the LQB/EBL interface. We adjust the Al composition in the insertion layer to alter the electrical polarity of the polarization-induced sheet charges, thereby modifying the electric field distribution in the EBL, LQB, and inserted GQB structure. Consequently, holes acquire boosted energy during their migration towards the active region. In addition, we enhance the hole injection and electron confinement ability via reducing the effective valence band barrier height and increasing the effective conduction band barrier height, thus diminishing the possibility of electron leakage from the active region into the p-type region. Therefore, the GQB structure proposed in this study provides a promising approach to improving the optical and electrical performance of DUV LEDs.

Isolated red quantum wells with strain relaxation induced by V-pits and trench structures

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Optics Express
https://doi.org/10.1364/OE.542926

Carrier localization leads to efficient emission in InGaN/GaN multi-quantum wells (MQWs), especially in the long-wavelength range. Nanostructures in MQWs can facilitate the formation of carrier localization centers. In this work, high-density V-pits and trench structures were introduced in MQWs by constant low-temperature growth. Isolated red MQWs were achieved due to the carrier blocking effect caused by the V-pits and trench structures. Meanwhile, the V-pits and trench structures caused significant stress relaxation in MQWs. The topmost quantum wells (QWs) achieved red emissions due to the composition-pulling effect, while the bottom QWs exhibited green emissions. In electroluminescence measurement, a single red emission peak appeared at 636 nm at 0.1 A/cm2. Temperature-dependent photoluminescence (PL) results showed that the PL integral intensity of the red MQWs at room temperature is about 11.32% of that at 6 K, while that of the green MQWs is only 0.09%. The PL lifetime for red emissions was more than 20 times longer than that for green ones. This study presents a new method to achieve carrier localization in red MQWs to minimize defect-related effects.

AlN-based vacuum ultraviolet Schottky barrier photodetector

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Optics Express
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Vacuum ultraviolet (VUV) photodetectors are essential for applications in space science, semiconductor lithography, and life science. In this study, we present what we believe to be a novel AlN-based VUV Pt-AlN Schottky barrier photodetector fabricated on a sapphire substrate. This device comprises an i-AlN/n-AlGaN layer structure and ingeniously utilizes an n-AlGaN layer and metal to establish an ohmic contact, addressing the challenge of n-type doping in AlN. Experimental results demonstrate a peak response of 0.06A/W at 194 nm under 0 V bias and clear rectification characteristics. The specific detectivity D* is 4.8 × 1012cm · Hz0.5 · W−1 at 0V bias for the device, indicating the device's excellent detection

performance. The realization of this device opens up possibilities for developing chip-level integrated detectors suitable for VUV detection.

Photoluminescence intensity enhancement of nanorod micro-LEDs via localized surface plasmon coupling

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Journal of Physics D: Applied Physics
https://doi.org/10.1088/1361-6463/ad9286

Nano-light-emitting diodes (LEDs) are ideal for ultra-high resolution displays due to their small size and high pixel density. However, traditional photolithography techniques fall short in meeting the requirements for nanoscale LED fabrication. Besides, as the size decreases and the specific surface area increases, non-radiative recombination generated by sidewalls defects becomes a significant issue, affecting the efficiency of nano-LEDs. To address this challenge, a nano-LED array with a single nanorod size of 800 nm was fabricated in this work by using nanosphere lithography and etching technology. Meanwhile, localized surface plasmons (LSPs) coupling technology was employed to enhance the PL efficiency of these nano-LEDs. By comparing with bare nano-LEDs, the PL intensity was boosted by about 43% and 129% when Ag and Ag@SiO2 nanoparticles were added separately. The existence of LSPs coupling process has been further confirmed through time-resolved photoluminescence measurement and finite element simulation analysis of different samples. The results provide compelling evidence for the LSPs coupling technology in enhancing the efficiency of nanoscale LEDs.

Polarization enhanced GaN separate absorption and multiplication ultraviolet avalanche photodiodes with an ScGaN interlayer

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Optics Letters
https://doi.org/10.1364/OL.541461

This article proposes a separate absorption and multiplication (SAM) GaN-based avalanche photodiode (APD) that achieves both high gain and low operating voltage by applying Sc-based ferroelectric material ScGaN in APDs. The avalanche gain of the proposed SAM APD with a low Sc composition p-ScGaN insertion layer reaches 7.2 × 104, which is 60% higher than that of a conventional p-i-p-i-n GaN-based APD. This improvement can be ascribed to the enhanced carrier transport properties induced by the polarization electric field. Meanwhile, the operating voltage is reduced from 77 V to 72 V. Furthermore, as the insertion layer has a significant impact on the internal electric field intensity and the band structure in APD devices, the doping concentration and thickness of the interlayer are optimized. The proper utilization of low Sc composition shows low lattice mismatch and high polarization, indicating the potential for further applications of ScGaN in photoelectric devices in the future.

Membrane thickness dependence of the suspended mini-LED on visible light communication

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Optics Express
https://doi.org/10.1364/OE.541456

This study proposes a suspended thin-film blue light emitting diode (LED) device using backside processing

to enhance the performance and light extraction efficiency (LEE) of silicon-based GaN LEDs. Photolithography, deep reactive ion etching (DRIE), and inductively coupled plasma (ICP) techniques were used to completely remove the silicon substrate, creating three LEDs with different GaN epitaxial layer thicknesses (5, 4.5, 4 µm). Compared to LEDs without ICP etching, the 5-minute etched LED exhibited superior optoelectronic performance, with current increasing from 75 mA to 99 mA at 3.5 V and peak light intensity 1.3 times higher at 50 mA. The 10-minute etched LED excelled in light-emitting efficiency and visible light communication (VLC), with a clearer eye diagram, highlighting its potential for high-performance VLC applications.

Experimental Evaluation of The Response of AlGaN/GaN UV Photodetectors with Square and Hexagonal Nanohole Arrays

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IEEE Sensors Journal
https://doi.org/10.1109/JSEN.2024.3502652

This study presents an experimental investigation of AlGaN/GaN ultraviolet photodetectors incorporating square and hexagonal nanohole arrays, aiming to enhance the devices' optical and electrical performance. The nanoholes were fabricated on the AlGaN surface using an etching process to improve light trapping and absorption across the UV spectrum. The study systematically compares the performance of square and hexagonal nanohole arrays against conventional planar devices. The results show that nanohole arrays significantly enhance UV photodetection, with square and hexagonal nanohole arrays exhibited superior responsivity of ~ 2 × 10 5 A/W at 365 nm, outperforming planar devices. Additionally, the hexagonal arrays demonstrated a higher UV/visible rejection ratio of 12, compared to 10 for square arrays and 4 for planar devices. This performance improvement is attributed to the optimized surface-to-volume ratio and light coupling efficiency provided by the nanostructures. While an increase in response times was observed in nanostructured devices, the overall enhancement in responsivity indicates the strong potential of nanohole arrays for improving UV photodetector efficiency. These findings demonstrate the feasibility of using nanostructuring techniques to advance wide-bandgap semiconductor photodetectors.

Correlation between recombination dynamics and quantum barrier thickness in InGaN-based MicroLEDs

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IEEE Photonics Journal
https://doi.org/10.1109/JPHOT.2024.3506779

To tackle the efficiency droop, we employed an epitaxial structure engineering approach and utilized SimuLED software to thoroughly investigate the influence of the quantum barrier (QB) thickness on the performance of Micro-LEDs, and delve into the corresponding carrier transport behavior. The results demonstrate that the effect of QB thickness on the performance of Micro-LEDs is closely related to injection current density. Within the current density range of 0–30 A/cm², a thicker QB layer leads to a higher internal quantum efficiency (IQE) for Micro-LEDs. Conversely, when the current density is in the range of 30–100 A/cm², employing a thinner QB layer in the LED structure can yield higher IQE values. In addition, this work suggests that tunneling effects and Quantum Confined Stark Effect (QCSE) dominate at different current densities, resulting in an opposite dependency of IQE on QB thickness. Furthermore, our findings indicate that adjusting QB thickness can significantly affect both the peak external quantum efficiency (EQE) and peak current density of Micro-LEDs.

Photon counting marine LiDAR using blue laser diode excitation

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Optics Express
https://doi.org/10.1364/OE.543523

Gallium nitride (GaN) laser diodes are shown to offer a viable alternative to the solid-state lasers typically used in photon counting ocean LiDAR. With their ability to operate at various blue wavelengths, coupled with compactness and efficiency, they offer some considerable advantages over conventional solid-state sources.

Interface Engineering of Rare-Earth Oxide-GaN Heterojunction for Improving Vacuum-Ultraviolet Photodetection

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IEEE Transactions on Electron Devices
https://doi.org/10.1109/TED.2024.3499945

Lutetium oxide (Lu 2 O 3), an ultrawide bandgap (UWB) (5.5–6.2 eV) rare-Earth oxide, has been proposed as a potential material for constructing vacuum-ultraviolet (VUV) photodetectors. In this work, an ultrathin (4 nm) aluminum oxide (Al 2 O 3) layer is deposited at the interface of Lu 2 O 3 /GaN heterojunction to fabricate a Lu 2 O 3 VUV photovoltaic detector with high performance. At 0 V bias and under VUV illumination, the Lu 2 O 3 /Al 2 O 3 /GaN photodetector presents a photoresponsivity of 17.2 mA/W (at 192 nm), a decay time of 54.9 ms, and a detectivity of 1.2 × 10 12 Jones. The excellent performance of the device comes from the ultrathin Al 2 O 3 layer deposited at the heterojunction interface, which not only acts as a buffer layer but also as a hole-blocking layer, improving the quality of the photosensitive layer and the separation efficiency of photo-generated carriers. Furthermore, with an increase in the thickness of the Al 2 O 3 layer (> 4 nm), a deterioration of optoelectronic properties of the Lu 2 O 3 /Al 2 O 3 /GaN device can be observed, which is attributed to an increase in the transport distance of the photo-generated carrier and a reduction in the probability of electron tunneling. This work can provide a reference for the preparation of high-performance Lu 2 O 3 -based VUV photovoltaic detectors in the future.

Effect of the self-aligned etching thin p-GaN layer on the performance of AlGaN-based DUV LEDs with various chip sizes

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Optics Express
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The light extraction efficiency (LEE) for deep ultraviolet light-emitting diodes (DUV LEDs) is significantly sacrificed by the absorption of the p-GaN layer. In this work, the self-aligned etching process is employed to laterally over-etched periphery thin p-GaN under the p-electrode by 10 μm to further improve the performance of AlGaN-based LEDs with various chip sizes. We find that when compared with reference devices with chip sizes of 40 × 40 μm2, 60 × 60 μm2 and 100 × 100 μm2, the optical power levels for the proposed DUV LEDs are enhanced by 16.66%, 11.41% and 7%, respectively. The most optical power enhancement can be obtained for the 40 × 40 μm2 DUV micro-LED chip. Hence, it is indicated that the laterally over-etched p-GaN design is more effective in increasing the LEE for DUV LEDs with reduced chip size. This shows the potential of the self-aligned etching p-GaN process in enhancing the LEE of DUV micro-LEDs. In addition, the lateral over-etched thin p-GaN suppresses the carrier diffusion to the device edge, which reduces the diffusion capacitance therein, hence leading to an increased −3 dB bandwidth to 55.4 MHz from 75.9 MHz for the packaged device of 100 × 100 μm2.

Dual-functional GaN photodiode for photodetection and neuromorphic computing with high specific detectivity

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Optics Letters
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The discrepancy in the photoresponse characteristics between photodetectors (PDs) and photosynapses is posing a challenge for integrating the two functions into a single device. In this work, a photodetector integrated with neuromorphic capabilities is demonstrated. Under the joint action of the photovoltaic effect and photoconductive effect, the proposed device can switch between the photodetector and photosynapse by simply altering the polarity of bias voltage. Under a reverse or zero bias voltage, the device operates as a photodetector with low dark current and high specific detectivity. On the other hand, when a positive bias voltage is applied, the device showcases synaptic functionalities such as excitatory postsynaptic current, paired-pulse facilitation, and transition from short-term memory to long-term memory. The dual-functional devices hold promise for weak light detection and neuromorphic computing in complex environments.

Photonic properties of InGaN-based micro-LEDs in the cryogenic temperature regime

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Optics Express
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InGaN/GaN-based micro LEDs ranging from 2 to 100 microns were characterized at cryogenic temperatures to reveal their temperature-dependent photonic properties. An atomic layer deposition technique was applied to passivate the sidewall of the device to enable photon emission of the 2-micron micro LEDs. The size-dependent Shockley-Read-Hall coefficients are extracted via the external quantum efficiency measurements under different temperatures. The micro LEDs' numerically fitted surface recombination velocity can be as low as 117.85 cm/sec. The emission peak photon energy revealed a non-monotonic variation across the 80 K-300 K temperature range. This behavior closely resembles the S-shaped temperature dependence of the emission peak due to carrier distribution in localized states in InGaN active regions. This localization effect, however, would be reduced when the injected current level increases and the temperature increases beyond 200 K.

High-Responsivity Flexible InGaN/GaN MQWs Nanomembrane Photodetectors with DBR Mirror towards Visible Light Communication

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IEEE Electron Device Letters
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Flexible InGaN-based photodetectors have broad application prospects in wearable biometric monitoring and visible light communication (VLC). However, flexible InGaN-based visible light photodetectors (VLPDs) still face challenges of low responsivity due to poor material quality and low light absorption efficiency. This work demonstrates a high-performance flexible VLPD integrating a TiO 2 /SiO 2 distributed Bragg reflector (DBR) mirror with an InGaN/GaN MQWs nanomembrane. The optical field density is significantly enhanced by introducing the DBR mirror, resulting in a 22% improvement in PD's responsivity (68.6 mA/W@-1 V). The photoresponse time (T r /T f) of PD are 24.4 μs and 6.1 μs, respectively. The -3 dB bandwidth of PD is 106.2 kHz. The flexible PD exhibits good stability over multiple bending cycles and long periods in the air. A real-time and precise VLC system link has been established based on high-performance flexible PDs, achieving a data rate of 9 Kbps. This research offers a strategic approach for

designing high-performance flexible VLPDs towards VLC.

Impact of Mg-Doped AlGaN Electron Blocking Layer on Micro-LEDs: A Comparative Analysis of Carrier Transport Versus Chip Size and Current Density

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IEEE Transactions on Electron Devices
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Micro-light emitting diode (micro-LED) is an essential component for the next-generation self-emissive display. However, existing studies often focus on specific parameters, such as chip size and current density, which restricts the overall understanding of micro-LEDs. This study presents a novel and extensive numerical analysis evaluating the impact of Mg-doped AlGaN electron blocking layers (EBLs) on InGaN-based micro-LED performance, covering current densities from 0.1 to 1000 A/cm 2 and mesa sizes from 3 to 100 μ m for micro-LEDs to > 200 μ m for conventional LEDs. Unlike prior studies, our work uniquely investigates the interplay between EBL doping concentrations and micro-LED performance across multiple dimensions, providing new insights into carrier injection mechanisms. By varying the EBL doping levels (1 × 10 19 cm −3 , 3 × 10 18 cm −3 , and without EBL), we explored their impact on the band alignment at the last quantum barrier (LQB) and EBL interface, which is crucial for modulating carrier injections and increasing light output power density (LOPD). The results indicate that optimizing EBL properties improves electron blocking at low current densities and enhances hole injection at higher densities, effectively reducing the current leakage and enhancing the luminous efficiency of micro-LEDs across a broad range of current densities. This comprehensive analysis challenges conventional micro-LED design approaches by emphasizing the importance of EBL engineering to achieve balanced and efficient carrier injections under a variety of operating conditions, providing a pathway for future innovations in micro-LED technology.

Ultrastable and Quick Response UV Photodetector by High Crystalline Orientation Wurtzite/Zinc-Blende GaN Superlattice

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Advanced Optical Materials
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1D gallium nitride (GaN) nanowires (NWs) can combine the intriguing properties of 1D materials with the wide bandgap nature of GaN materials. In this study, a type of high crystalline orientation wurtzite (WZ)/zinc-blende (ZB) superlattice (SL) NWs is synthesized for the first time to the knowledge, which special structure can be also demonstrated by first-principles calculation. The proposed GaN SL NWs UV PD demonstrates pronounced photoelectric performances working in a self-powered mode, including a large responsivity (23.72 mA W−1), a high specific detectivity (4.4167 × 1011 Jones), and a fast response speed (rise/decay time of 0.76/0.8 ms, significantly better than most of the gallium series NWs photodetectors reported so far). And the PD also exhibits excellent stability, enabling the photocurrent to remain largely consistent over a period of 18 months, which photoelectric current decay rate is less than 1%/year. These outstanding performance of WZ/ZB GaN SL NWs may be benefited from more stable structure and their diverse electronic channeling of GaN SL surface distributed gold quantum dots compared to that of pure WZ or ZB phase GaN. This research shows WZ/ZB GaN SL NWs' exceptional UV PD performance and new insights into their electronic structures for device applications.

Optical Investigations of Nano-LEDs Based on Submicron-Sized III-Nitride Platelets

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physica status solidi b
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A study of submicron-sized InGaN containing a single quantum well, intended for use as nano-light-emitting diodes in high-resolution display based on direct emission, is presented. Herein, the structures are grown by a bottom-up method from holes in a masked GaN/sapphire substrate and are intended for red emission. Many of the platelets show dark lines in cathodoluminescence images, previously identified as stacking mismatch boundaries. These introduce local shifts in the reduced emission, perhaps related to local strain. However, the total emission position stays unaffected, just reduced in intensity. Due to an unintended variation in the size of the c-facet, there is a gradient in the indium content which, in turn, leads to a significant shift in the peak position of the quantum well emission. With increasing probe current there is a slight blueshift, likely a result of the quantum confined Stark effect.

Sputtered aluminum nitride waveguides for the telecommunication spectrum with less than 0.16 dB/cm propagation loss

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We report the fabrication and characterization of photonic waveguides from sputtered aluminum nitride (AlN). The AlN films were deposited on 6” silicon substrates with a 3 µm buried silicon oxide layer using reactive DC magnetron sputtering at a temperature of 700°C. The resulting uncladded polycrystalline waveguides exhibit propagation losses of 0.137 ± 0.005 dB/cm at wavelengths of 1310 nm and 0.154 ± 0.008 dB/cm at a wavelength of 1550 nm in the TE polarization. These results are the best reported for sputtered AlN waveguides in the C-band and the first report in the O-band. These performances are comparable to those of the best-reported AlN waveguides, which are epitaxially grown by metal-organic chemical vapor deposition (MOCVD) on sapphire substrates. Our findings highlight the potential of sputtered AlN for photonic platforms working in the telecom spectrum.

Demonstration of UV-A stimulated emission from optical pumping with a nano-porous cladding layer

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Applied Physics Express
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We report a room-temperature ultraviolet-A (UV-A) stimulated emission from a multiple-quantum-well laser diode featuring a nano-porous bottom cladding layer on the GaN substrate. For a 1500×15 µm ridge-type edge-emitting laser, we achieved a 372.8 nm emission under optical pumping, with a full-width-half-maximum (FWHM) of less than 2 nm and a threshold optical pumping power density of less than 1.2 MW cm−2. The integration of a nano-porous cladding layer effectively minimizes lattice mismatch, enhances confinement factor, and maintains electrical conductivity. This demonstration expands the potential for developing high-performance UV laser diodes on GaN substrates, overcoming limitations previously imposed by critical thickness contrasts.

InGaN/GaN edge emitting laser diodes using an epitaxial lateral overgrowth with a low-defect density area of more than 75%

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We have successfully demonstrated InGaN/GaN edge-emitting laser diodes (EELDs) on a fully coalesced epitaxial lateral overgrown film from a c-plane GaN substrate. We achieve a high aspect ratio, low defect density wing region covering 75% –88% of the substrates' surface, which is amongst the largest reported area in the literature. The devices at the wing region exhibit a threshold current density of 3.63 kA/cm² at 408 nm, and an improved laser performance compared to the high defect density region is confirmed. Based on this work, it is promising that high performance, cost-efficient c-plane InGaN/GaN EELDs can be realized.

High-Temperature Ultraviolet Photodetector and Amplifying Integrated Circuits Based on AlGaN/GaN Heterostructure

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In this work, an ultraviolet (UV) photodetection and amplifying integrated circuit (IC) based on an AlGaN/GaN heterostructure is demonstrated. The IC consists of a metal-heterostructure-metal photodetector (MHM-PD) and a high-electron-mobility transistor (HEMT)-based amplifier. The photoresponse of the MHM-PD increases at elevated temperatures due to the spatial separation of the photocarriers under the polarization electric field at the AlGaN/GaN heterointerface, as well as the photo-enhanced leakage current through the metal-heterostructure junction. At 250 ℃, MHM-PD achieves a peak photoresponsivity of 14.5 A/W and a UV-to-visible rejection ratio of 104. As the thermal chuck temperature increases from 25 ℃ to 250 ℃, the performance of the HEMT-based amplifier shows good thermal stability. Finally, the IC achieves a photoresponse of over 106 V/W and a switching frequency of 50 kilohertz at 250 ℃ with rise and decay time constants of 3.95 µs and 2.8 µs, respectively. These results show that the IC has a high-sensitivity and high-speed UV detection capability.

Rejection Ratio and Responsivity of Dual-Layer III-Nitride Alloy Photodetectors

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The III-Nitride alloys (AlGaN and InGaN) photodetectors with Schottky barriers have been studied, focusing on two structures with active layers: one based on $Al_{0.25}Ga_{0.75}N$/GaN semiconductors and the other on an $In_{0.05}Ga_{0.95}N$/GaN heterostructure. For an overall efficiency of 70%, both proposed devices exhibit remarkable responsivity. The AlGaN structure achieves a responsivity of 111.25 A/W at 2V, while the InGaN device attains 4.302 A/W under the same voltage. At an applied voltage of 8V, the responsivity of the AlGaN device increases to 83.73 A/W, whereas the InGaN device reaches 34.42 A/W. When operating at 10V, the AlGaN structure demonstrates a responsivity of 105 A/W, in contrast to 6.84 A/W for the InGaN device. At room temperature, the visible rejection ratio for the $Al_{0.25}Ga_{0.75}N$/GaN device is 3.33×10^4 at 10V, a high value that indicates the superior performance of the $Al_{0.25}Ga_{0.75}N$ photodetector. In comparison, the $In_{0.05}Ga_{0.95}N$/GaN-based photodetector achieved a value of 2.935 at 10V.

Additionally, the maximum photocurrent obtained was 3.045 mA for the $Al_{0.25}Ga_{0.75}N$ device at 10V and 0.0472 mA for the $In_{0.05}Ga_{0.95}N$ device at the same voltage.

Red light-emitting diode with full InGaN structure on a ScAlMgO4 substrate

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Applied Physics Express
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Here, we report the first demonstration of a full InGaN-based red LED grown on a c-plane ScAlMgO4 substrate. This work represents a potential approach for achieving red emissions from an InGaN quantum well grown on InGaN underlying layers. The LED device exhibits a peak wavelength of 617 nm at a current injection of 40 mA (10.5 A cm−2). The light output power and external quantum efficiency were 12.6 μW and 0.016% at 40 mA (10.5 A cm−2), respectively. These results are expected to contribute to the development of longer-wavelength emission LEDs and laser diodes.

Failure analysis of GaN-based optoelectronic devices: Insights into photo-induced electrochemical migration

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GaN-based optoelectronic devices exhibit exceptional performance. However, the photo-induced electrochemical migration (PECM) effect poses risks to their long-term reliability, especially under light and humidity exposure. This paper explores the underlying causes of PECM, identifying environmental light, moisture, and the presence of metallic elements as key factors. This study reveals that the PECM-related surface insulation resistance (SIR) failure is driven by the formation of dendritic structures between the anode and cathode, with faster SIR failure observed as electrode spacing decreases. An in-depth description of the electrochemical migration process is provided.

Interfacial polarization charge engineering with co-designed LQB and EBL for enhanced EQE of AlGaN DUV LEDs

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Semiconductor Science and Technology
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In this paper, we propose to modulate the polarization charges at the interface between the last quantum barrier (LQB) and the electron blocking layer (EBL) via strategically adjusting the Al composition in the LQB and EBL simultaneously. With appropriate design of the linear gradient profile in Al composition, the original positive polarization charges at the LQB/EBL interface can be diminished or converted into negative charges, which helps to reduce the positive electric field in EBL, thus adjusting the energy band near the LQB/EBL interface. Enhanced effective barrier height for electrons, decreased effective barrier height for holes, and accumulation of a large number of holes at the LQB/EBL interface are obtained, resulting in improved electron leakage and hole injection. In comparison with the reference deep ultraviolet light-emitting diode (DUV LED), an enhanced external quantum efficiency (EQE) by 37.5% at an injection current density of 100 A/cm2 is achieved for the device with negative polarization charges. The modulation strategy of polarization charges at the LQB/EBL interface via co-designing the linear gradient of Al

composition in LQB and EBL can be a feasible approach for obtaining high-performance DUV LEDs.

Theoretical study of the temperature dependence of Auger-Meitner recombination in (Al,Ga)N quantum wells

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Non-radiative Auger-Meitner recombination processes in III-nitride based optoelectronic devices operating in the visible spectral range have received significant attention in recent years as they can present a major contribution to the efficiency drop at high temperatures and carrier densities. However, insight into these recombination processes is sparse for III-N devices operating in the ultraviolet wavelength window. In this work we target the temperature dependence of the Auger-Meitner recombination rate in (Al,Ga)N/AlN quantum wells by means of an atomistic electronic structure model that accounts for random alloy fluctuations and connected carrier localisation effects. Our calculations show that in the low temperature regime both the non-radiative Auger-Meitner and radiative recombination rate are strongly impacted by alloy disorder induced carrier localisation effects in these systems. The influence of alloy disorder on the recombination rates is reduced in the high temperature regime, especially for the radiative rate. The Auger-Meitner recombination rate, however, may still be more strongly impacted by alloy disorder when compared to the radiative rate. Our calculations show that while on average radiative recombination slightly increases with increasing temperature, the Auger-Meitner recombination process may, on average, slightly decrease in the temperature range relevant to the thermal efficiency drop (thermal droop). This finding suggests that the considered Auger-Meitner recombination process is unlikely to be directly responsible for the thermal efficiency drop observed experimentally in (Al,Ga)N/AlN quantum well based light emitting devices. Thus, different non-radiative processes, external to the active region, may be the underlying cause of thermal droop in (Al,Ga)N wells.

Enhanced performance of AlGaN solar-blind ultraviolet avalanche photodiodes through electric field optimization

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Micro and Nanostructures
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A back-illuminated AlGaN separate absorption and multiplication (SAM) solar-blind ultraviolet (UV) avalanche photodiode (APD) with an enhanced electric field is designed in this work. For the designed APD, a polarization electric field aligned with the applied electric field can be introduced by reducing the Al content of the p-type layer and inserting a multiplication layer with low-Al-content. The calculation results show that the designed APD exhibits a 9.6 V reduction in breakdown voltage, a 29 % increase in avalanche gain, and a 32 % improvement in peak responsivity at the breakdown voltage compared to the conventional SAM APD. In order to maximize the responsivity, further parameter optimization of the multiplication and p-type layers of the designed APD is performed using the Jaya algorithm. The results show that compared to the conventional SAM APD, the peak responsivity at the avalanche breakdown voltage and avalanche gain of the optimized APD are improved by 103 % and 63 %, respectively.

Influence of high-k La2O3 interfacial oxide layer on the performance of GaN based Schottky barrier ultraviolet-B and A photodetection sensors

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GaN based metal-semiconductor-metal (MSM) type Schottky heterojunction-based ultraviolet (UV) photodetectors (PDs) have already proven as an efficient candidate for photodetection applications. However, in real time applications, GaN based MSM type UV PD device display higher dark current, weak signal detection and required external bias are seriously limiting their usage. Therefore, self-powered interdigitated electrode type Cr/Cu/La2O3/GaN: MIS (metal-insulator-semiconductor) heterojunction visible blind UV PD has been fabricated and studied in UV-B and A region. The structure, morphology, chemical and optical parameters of La2O3 films were evaluated using GIXRD, AFM, XPS and UV–Vis techniques, respectively. The reported interdigitated Cr/Cu/La2O3/GaN: MIS UV PD device yielded a higher Schottky barrier height (SBH) of 0.95 eV (dark) and 0.89 eV (360 nm) indicating the formation of higher potential barrier. At an applied bias of 0 V, the fabricated GaN MIS PD yielded an UV to visible rejection ratio (R360/R400) of 1.62 × 102. In UV-A region (at 0 V of 360 nm), the fabricated Cr/Cu/La2O3/GaN: MIS UV PD device exhibited a peak responsivity of 28.9 mAW−1, D∗ of 3.57 × 1012 Jones and EQE of 19.2 %. On the other hand, in UV-B region (at 0 V of 310 nm) the MIS UV PD device exhibited a peak responsivity of 34.4 mAW−1, D∗ of 4.2 × 1012 Jones and EQE of 22.7 %. During 360 nm illumination (at 0 V), the temporal response measurements of GaN UV PD device yielded the best rise/fall times of 70 ms/141 ms. This work validates the fact that the high-k La2O3 thin film as an interfacial oxide layer at the metal/GaN interface provides a novel solution for the photo detection field in the self-powered mode i.e., without any external bias.

Bandwidth optimization of GaN-MQW photodetectors for visible light communication via deep etching and bias voltage control

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Optics & Laser Technology
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In pursuit of an all-in-one chip for simultaneously working as a transmitter and a receiver of visible light communication (VLC) system, there has been a surge in research that employs GaN multiple quantum well (MQW) epitaxial structures as a photodetector (PD) but a lack of comprehensive research of the bandwidth of GaN-MQW PD. In this paper, we investigated the effects of deep etching and shallow etching processes, as well as bias voltage, on the bandwidth of the PD. The results show that the deep etching process significantly reduces the device capacitance to a minimum of 0.294 pF, thereby removing the limitations of the RC effect on the bandwidth. Meanwhile, without the constraints of the RC effect, the bandwidth increases exponentially with the increase in bias voltage, without significantly reducing the signal-to-noise ratio of the system. Under the conditions of deep etching and high bias voltage, a record-breaking-level bandwidth of 914.475 MHz and a high communication data rate of 12.615 Gbps are achieved. This study guides the analysis and enhancement of the bandwidth for GaN-MQW PDs

and validates the tremendous potential of GaN-MQW PDs as receivers for VLC systems.

Enhancing Ni/Cr/n-GaN Schottky junction performance using a novel Bi2O3 insulating layer for advanced optoelectronic device applications

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Bismuth oxide (Bi2O3) insulator layer was used to prepare a Ni/Cr/Bi2O3/n-GaN Metal-insulator-semiconductor (MIS)-type junction. X-ray diffraction (XRD), scanning electron microscopy (SEM), X-ray photoelectron spectroscopy (XPS), current–voltage (I-V), and capacitance–voltage (C-V) techniques were used to examine the junctions structural, chemical, and electrical properties. XRD, and SEM findings indicated that the Bi2O3 films exhibited a high-quality interface between metals and n-GaN substrate. The XPS depth profile shows a list of elements within the prepared MIS junction. Ni, Cr, Ga, O, N, Ti, Bi, and Al are among the elements in this junction. The significant concentration of these elements stands out notably in both the interfacial layer and the metal electrodes on n-GaN substrate. Remarkably, the prepared MIS junction exhibited superior rectifying behavior coupled with reduced reverse leakage current when compared with the Ni/Cr/n-GaN Metal-Semiconductor (MS) junction. The calculations demonstrated that the MIS junction exhibits a higher barrier height (1.18 eV) and ideality factor (1.32) compared to the MS junction, which has a barrier height of 0.84 eV and an ideality factor of 1.15. These results indicate that the Bi2O3 insulating layer significantly modifies the electrical properties of the prepared junction. Utilizing various methodologies, including Cheung's, Norde functions, ΨS-V, and Hernandez plots, barrier heights, ideality factor and series resistance were estimated and found to be consistent with each other. The Bi2O3 interlayer has demonstrated its effectiveness as a high-quality insulating material, making it an excellent candidate for the fabrication of GaN-based MIS junctions. Its presence enhances the device's electrical properties, providing superior insulation and optimizing interface performance for advanced optoelectronic applications.

On-chip integrated plasmon-induced high-performance self-powered Pt/GaN ultraviolet photodetector

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Chip
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The advantages of on-chip integrated photodetectors, such as miniaturization, high integration, and reliability, make them an indispensable and important part of electronic devices and systems. Herein, we experimentally exhibit a monolithically integrated

ultraviolet photodetector utilizing GaN microcylinder epitaxial-structure on Si wafer, with its photoresponse properties plasmonically-boosted using Pt nanoparticles via specific sizes. When illuminated upon ultraviolet light at 0 V bias, the Pt/GaN device has significant photovoltaic performances, including a peak responsivity of 200.1 mA W-1, external quantum efficiency of 65% and other figures-of-merit. Finite element analysis and energy band theory confirm that the excellent photodetection properties of the Pt/GaN device are related to the strong plasmon absorption and the increase of hot electrons injected into the GaN conduction band, which make its photoresponse performance and robustness in application much better. To realize the multipurpose capability of the devices, we validate the application of Pt/GaN as turbidity sensing and achieve a resolution of up to 100 NTU. Moreover, the prepared devices can be used as optical data receivers for optical communication. These findings provide references for on-chip detectors to improve overall system performance and drive the realization of more complex applications.

Temperature dependent low-frequency noise characteristics of AlGaN avalanche photodiodes with ultra-shallow bevel edge termination

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In this work, temperature dependent low-frequency noise characteristics of Al0.1Ga0.9N p-i-n avalanche photodiodes (APDs) with ultra-shallow bevel edge termination were studied. Benefiting from the termination, the sidewall leakage current of the APDs is extremely low, thus reducing the surface noise, which is critical to explore the origin and effect of traps inside the devices. The results show that 1/f noise and generation-recombination (G-R) noise dominate the noise spectra at low reverse bias, G-R noise becomes stronger with increasing reverse bias, and finally, avalanche excess noise becomes dominant under the avalanche state. The fabricated Al0.1Ga0.9N p-i-n APDs present low noise with a minimum equivalent noise power of 3 × 10−13 W. Additionally, the random telegraph signal (RTS) noise is found and a trap level is extracted to be about 0.53 eV, both of which contribute to G-R noise. Further, the unusual current- and temperature-dependent characteristics of low-frequency noise are discussed in detail, which are attributed to the dominant carrier transport mechanisms transiting from hopping conduction to tunneling process. The obtained results are of great significance for the structure design and reliability assessment of Al0.1Ga0.9N p-i-n APDs.

Ultra-sensitive broadband photoresponse realized in epitaxial SnSe/InSe/GaN heterojunction for light adaptive artificial optoelectronic synapses

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By integrating sensing, memory, and computing functions within a single unit, the neuromorphic device enables brain-like computing that could facilitate artificial intelligence applications due to its superior scalability and efficiency. As an emerging form of neuromorphic devices, optoelectronic synapses for artificial visual perception with high optical sensing performance and tunable memory time are highly desired. Herein, we report a new design of ultra-sensitive broadband artificial optoelectronic synapses based on a tailored hybrid heterostructure of epitaxial SnSe/InSe/GaN multilayers, in which the interlayer InSe has been employed as the functional layer. Specifically, InSe plays the crucial role of charge trapping layer by blocking the thermally excited carriers in the potential well, thus an ultra-low dark current in 10−10 A level has been realized under the bias of −1.5 V. Moreover, the InSe layer could significantly extend the photocurrent decay time, which enabled the synaptic functions in the devices. Such multilayer heterojunctions exhibit a broadband photoresponse spanning from the near-infrared to the ultraviolet, with a specific detectivity up to 1.07×1011 Jones under 365 nm excitation. Combining all these

merits, light adaptive artificial optoelectronic synapses with multi-color stimuli perception capability have been demonstrated. These results provide a novel and promising strategy for future applications in artificial vision systems.

Investigation of ultrasmall sidewall-insulated GaN via with large aspect ratio for the strategy of vertically stacked full-color Micro-LEDs

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Optics Communications
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Micro light-emitting diode (Micro-LED) is considered as an ideal candidate for near-eye, outdoor display, and light field photography applications. At present, the commercialization of full-color Micro-LED is limited by the mass transfer of red, green, and blue (R-B-G) sub-pixels. Hence, we proposed a full-color scheme of vertically stacked tricolor Micro-LED layers to avoid mass transfer, which owns over 1000 PPI (pixel per inch). In this solution, the sidewall-insulated via in the epilayer plays a critical role to achieve the electrical and mechanical integration of three monochromatic Micro-LEDs with Si-based complementary metal-oxide semiconductor (CMOS) driver. Therefore, the via processes of GaN-based epilayer were investigated systematically using available semiconductor processes in this article. The inductively coupled plasma (ICP) etching was employed to create the ultra-small micro-structure array using SiO2 thin film as hard mask. Sidewall-insulated vias were fabricated with different aperture sizes (9.3, 7.5, and 3.4 μm) and a depth of about 4-μm. The vias with large aspect ratio are completely satisfy the requirement of designed vertical interconnection. This study aims to provide valuable reference for the commercial progress of high-resolution and full-color Micro-LEDs.

Active-matrix TFT driven GaN blue Micro-LED display realized with electroplated copper-tin-silver micro bumps-based bonding structure

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With the rapid advancement of display and smart lighting technologies, micro-light-emitting diodes (Micro-LEDs) have garnered substantial attention due to their exceptional performance characteristics. However, a significant challenge persists in achieving reliable interconnections between Micro-LED chips and driver backplanes. This article proposes and implements the Double-Layer Photoresist Structure Electroplating (DPSE) technique for fabricating Cu-SnAg metal bumps, thereby facilitating the heterogeneous integration of oxide thin film transistors (TFTs) with GaN-based blue LEDs. The DPSE process was optimized by addressing several critical factors, including the correlation between bump height and electroplating time, the occurrence of cracks in the photoresist surface, and the removal of the conductive layer. Metal bumps were successfully fabricated on TFT backplanes with dimensions of 16.5 μm × 10 μm, an average height of 5.39 μm, and a uniformity of approximately 2.266 %. To demonstrate the efficacy of this approach, a 0.495-inch blue active-matrix Micro-LED display was designed and fabricated. This display features a mesa size of 15 μm × 30 μm, a pixel pitch of 222 μm, and a pixel density of 114 pixels per inch (PPI). The resultant blue Micro-LED display exhibits excellent optical characteristics, achieving a brightness of 1625 cd/m² (nits). It is anticipated that the methodology and findings presented in this study will contribute significantly to the advancement of

Micro-LED display technology in consumer electronics. This research not only represents a significant advancement in the field of Micro-LED display technology but also paves the way for future innovations in high-resolution, energy-efficient display systems.

Study on the fabrication of UV LED based on Au/i-AlN/n-GaN structure and the effect of operating temperature on the carrier transmission and electroluminescence characteristics

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GaN-based light-emitting diodes (LEDs) have important applications in medical diagnostics, sterilization, and other fields. However, the mismatch of p-type materials usually makes it difficult for conventional pn-type GaN-based LEDs to obtain pure ultraviolet (UV) emission. In this paper, a series of metal-insulator-semiconductor (MIS)-type diodes with Au/i-AlN/n-GaN structure were prepared by varying the deposition time of AlN films, and the effects of ambient temperature on their electrical and electroluminescence (EL) properties were investigated. The Au/i-AlN/n-GaN diode achieved high-purity UV emission, and the device had the lowest turn-on voltage and the strongest EL intensity when the deposition time of AlN is 40 min. In addition, the effect of ambient temperature on the EL performance of the MIS-type LED was investigated, and the emission was attenuated due to thermal effects at temperatures above 40°C. Finally, we clarified the source of holes from the energy band structure and discussed the luminescence mechanism of the device. The results show that the MIS structure is an attractive choice to effectively realize the UV emission of GaN-based LEDs.

Low current driven blue-violet light-emitting diodes based on p-GaN/i-Ga2O3/n-Ga2O3:Si structure

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Optics & Laser Technology
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This paper reports a low current driven LED with p-GaN/i-Ga2O3/n-Ga2O3:Si structure prepared by radio frequency (RF) magnetron sputtering, the driving current of the device is only 0.02 mA. Compared with the reported drive current of the LEDs, the reduction is 100 or even 1000 times. Through the study of its electrical properties, it was found that it had excellent rectification characteristics at different ambient temperatures and the turn-on voltage was about 1.8 V. In addition, the leakage current was as low as 4.30 × 10-8 mA. Through the electroluminescence test, it was found that the device had the function of emitting in the ultraviolet (363 nm) and visible (425 nm) region, which realized the blue-violet luminescence at room temperature. Furthermore, the device had excellent high temperature color stability and ultra-low color temperature of 1924 K. The color coordinate of the device at room temperature was (0.1905,0.0955). A detailed study was conducted on the electroluminescence mechanism of the device through its band structure, and the causes of the luminescence were analyzed through the Gaussian fitting of the EL spectrum.

The impact of barrier modulation on carriers transport in GaN quantum well infrared detectors

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Micro and Nanostructures
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GaN quantum well infrared detectors are affected by the epitaxy process and the polarization electric field within the quantum well, making it difficult to fabricate actual devices and regulate their performance. This study utilized the APSYS software to build a transport model for GaN quantum well infrared

detectors. Based on the optimal quantum well structure GaN/Al0.8Ga0.2N with an absorption peak wavelength around 1550 nm, the modulation of barrier width is used to elucidate the control of E1 energy level in the quantum well, as well as the variation patterns of absorption spectra for quantum well intersubband transitions(ISBT) and polarization electric fields. Under the influence of polarization electric fields, the devices exhibit completely opposite changes in current when subjected to positive and negative biases, respectively. By using Gauss transient spectroscopy, the influence of triangular barriers on the photoelectron transport on the E1 energy level was investigated, and it was determined that the optimal barrier width is 3 nm. At this width, the device exhibits the fastest relaxation within the well and transport between wells. By analyzing the AC impedance, the equivalent circuit of the device was obtained and the rationality of the circuit structure was demonstrated.

Highly integrated optocoupler based on monolithic III-nitride diodes for on-chip data transfer

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This letter reports a monolithic integration method for constructing a chip-scaled optocoupler. By integrating light-emitting diode (LED) and photodiode (PD) with the same multiple quantum well (MQW) structure on a single wafer, a highly integrated GaN-based optocoupler is obtained with a size of 2.6 mm x2.6 mmx0.1 mm. The device exhibits a fast response time with a rise time of 5.43μs and a fall time of 7.88μs, and a current transfer ratio (CTR) of 0.1% obtained at the injection current of 10 mA. In addition, by integrating this proposed optocoupler with wireless communication technologies, a remote control scheme for audio collection and processing is presented. Remarkably, a distributed Bragg reflector (DBR) coating on the sapphire surface greatly improves the on-chip detection ability. The proposed and demonstrated monolithically integrated, chip-scaled, cost-effective, wireless-compatible properties of the optocoupler may provide more potential application scenarios in optical interconnect systems.

3.65 W of 335 nm cw Generation In a Pr3+:LiYF4 Laser Pumped By a Fiber Coupled Blue LD Module

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We report on the stable 670/335 nm Pr3+:LiYF4 (Pr: YLF) continuous-wave (CW) laser. A fiber-coupled InGaN laser diode (LD) emitting at 444 nm is used as the pump source, effectively increasing the pump power. Using a straight cavity structure, we achieved a maximum output power of 7.4 W at 670 nm with a pump power of 37 W. Second-harmonic generation (SHG) of the 670 nm laser was achieved using a lithium borate (LBO) crystal. To avoid damage to the gain material by the UV laser, a V-folded cavity structure is adopted for intracavity frequency doubling. With an incident pump power of 32 W, more than 3.65 W was obtained at 335 nm with an optical-to-optical conversion efficiency of 11.4%, and the output power stability in one hour is better than 0.5%. To the best of our knowledge, this is the first research on Pr: YLF laser emitting at 335 nm. This research has high application value in fields such as photobiology and semiconductor detection.

Deep localization features of photoluminescence in narrow AlGaN quantum wells

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The research prepared two deep ultraviolet (DUV) AlGaN-based multiple quantum well (MQW) samples

with the same Al content in the QWs but different well widths (3 nm for Sample A and 2 nm for Sample B). Photoluminescence (PL) measurements reveal that Sample A exhibits only one main PL peak across all measured temperatures, while Sample B displays one main PL peak at low temperatures and two distinct PL peaks at high temperatures. Furthermore, compared with Sample A, Sample B exhibits a more significant temperature-dependent PL peak wavelength blue shift relative to the Varshni curve, a more significant excitation power density-dependent PL peak blue shift accompanied by linewidth broadening, as well as a larger non-radiative recombination related activation energy and higher internal quantum efficiency (IQE). These findings can be explained by the observation that the narrower well width of Sample B induces a more pronounced effect of carrier localization than the wider well width of Sample A, due to the enhanced fluctuation in well width and reduced quantum-confined Stark effect (QCSE).

Photoelectric characteristic of single-phase InxGa1-xN films with tunable bandgap through RF magnetron sputtering

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InxGa1-xN films with tunable bandgap hold significant potential for photoelectric applications, particularly in wavelength-selective and UV–visible photodetection. Herein, a unique target was designed to prepare bandgap-tunable InxGa1-xN films by RF (radio frequency) magnetron sputtering. By adjusting the RF power to change the In content (x value), we prepared InxGa1-xN films with bandgap variations in the range of 2.15–2.63 eV. Upon further investigation, it was found that the grown InxGa1-xN films had hexagonal structure and did not undergo phase separation in the In-rich composition. With the increase of In content from 0.46 to 0.60, the preferred orientation of the InxGa1-xN films changed from (101) to (100) plane, while the surface morphology of the InxGa1-xN films changed from worm-like to spherical grains. Photoluminescence peaks of InxGa1-xN films was composed of intrinsic and defect luminescence. Under irradiation of 450 and 650 nm laser, the responsivity of the InxGa1-xN metal–semiconductor-metal photodetector can reach 5.15 × 10−7 and 3.2 × 10−7 A/W, and the fastest response time can reach 1.28 and 1.32 s, respectively.

Silicon-based InGaN/GaN microbelt blue light-emitting-diode fabricated via low-temperature direct bonding

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Integrating nitride semiconductor light source on Si is a key to build wide-spectrum photonic systems, however, there have been many challenges to grow nitride semiconductors directly on Si substrate. Herein, freestanding InGaN/GaN-based microbelts were first prepared by electrochemical lift-off (ELO) technique from as-grown sapphire substrate. The obtained microbelts have uniform morphology and can be flexibly transferred. Subsequently, direct bonding technology was used to transfer and integrate the released InGaN/GaN-based microbelt onto high conductivity Si substrate to fabricate on-chip microbelt light-emitting diode (MBLED) with vertical injection structure. An intermediate amorphous layer with a thickness of ~ 25 nm was formed at the interface of GaN and Si, which was found having no obvious negative effect on the electrical injection of the MBLED. The prepared Si-based InGaN/GaN MBLED emitted a 465 nm light at the end face of microbelt with unidirectional luminescent waveguide properties. The luminescence intensity showed a high linear correlation with increasing current. Fowler-Nordheim tunneling (FNT) and thermionic emission (TE) were found to be responsible for the current transport mechanisms of it at low and high voltage, respectively. This study provides a simple, low-cost method for integrating III-V semiconductor devices on Si substrate.

Stacking-enabled Si/GaN tunnel junction light-emitting diodes with improved radiative recombination efficiency

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Improving carrier injection for radiative recombination in GaN light-emitting diodes (LEDs) has been a major focus for several decades. In this study, the performance of GaN LEDs was enhanced through the construction of an Si/GaN tunnel junction (TJ) via nanomembrane (NM) stacking. The n + Si nanomembrane was transfer printed onto the p + GaN layer, resulting in an n + Si/p + GaN TJ on top of the GaN epi-structure. The radiative recombination of electron–hole pairs was enhanced by the tunneling of carriers across the Si/GaN TJ into the InGaN/GaN multi-quantum wells. The improved hole injection was elucidated through the energy band diagram of the Si/GaN TJ. The increased number of injected holes in the stacked Si/GaN TJ LED leads to enhanced radiative recombination, resulting in greater output power and external quantum efficiency (EQE). Specifically, the light output power improved by 96% at 30 A/cm2, and the peak EQE increased by 36% due to the formation of the stacked Si/GaN TJ on the LED. These findings can be applied to the manufacturing of electronic devices, where balancing carrier generation and injection is crucial for operational efficiency.

Streamlined Algorithm for Two-dimensional Bandgap and Defect-state Energy Variations in InGaN-based Micro-LEDs

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Materials Horizons
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Bandgap and defect-state energy are key electrical characteristics of semiconductor materials and devices, thereby necessitating nanoscale analysis with a heightened detection threshold. An example of such a device is an InGaN-based light-emitting diode (LED), which is used to create fine pixels in augmented-reality micro-LED glasses. This process requires an in-depth understanding of the spatial variations of the bandgap and its defect states in the implanted area, especially for small-sized pixelation requiring electroluminescence. In this study, we developed a new algorithm to achieve two-dimensional mappings of bandgap and defect-state energy in pixelated InGaN micro-LEDs, using automated electron energy-loss spectroscopy integrated with scanning transmission electron microscopy. The algorithm replaces conventional background subtraction-based methods with a linear fitting approach, enabling enhanced accuracy and efficiency. This novel method offers several advantages, including the independent calculation of defect energy (Ed) and bandgap energy (Eg), reduced thickness effects, and improved signal-to-noise ratio by eliminating the need for zero-loss spectrum calibration. These advancements allow us to reveal the relationship between the bandgap, defect states, microstructure, and electroluminescence of the semiconductor under ion-implantation conditions. The streamlined analysis achieves a spatial resolution of approximately 5 nm and an exceptional detection limit. Additionally, ab-initio calculations indicate gallium vacancies as the predominant defects.

Prediction of impurity concentrations in AlN single crystals by absorption at 230 nm using random forest regression

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This study introduces a rapid and non-destructive impurity characterization method using UV absorption spectroscopy that is calibrated against secondary ion mass spectrometry (SIMS) data. A random forest regression model was evaluated for carbon, oxygen, and silicon impurity prediction based on absorption spectra. AlN boules were grown using the seeded PVT method with tungsten crucibles, processed into wafers, and characterized. A matrix of 37 samples with varying impurity concentrations in the range 1 × 1017 to 5 × 1019 cm−3 was created using element-specific doping methods. SIMS and absorption spectroscopy data revealed characteristic absorption patterns for different impurities. Absorption at 230 nm, which is a crucial wavelength for UVC-LEDs, correlated well with

the overall impurity concentration. The random forest model predicted impurity concentrations accurately when similar training data were available, but high prediction errors occurred for unique impurity profiles. To improve prediction accuracy, a more extensive sample series and/or more complex AI tools are required.

Correlated photoluminescence blinking phenomenon on InGaN/GaN nanopillar structures

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Light-emitting devices that take advantage of the wide bandgap characteristics of InGaN/GaN are widely used in the industry. However, inhomogeneities have been reported in their photoluminescence (PL) mapping at the nanometer and submicrometer scale, even in samples of high crystal quality. In addition, a blinking phenomenon (time variation of PL intensity) under photoexcitation has been reported in relation to these inhomogeneities. The reason why this blinking phenomenon occurs is still unclear; it has been observed in quantum dots and other single and multilayer quantum well structures. Nevertheless, there are very few publications on nanopillar InGaN quantum well samples, which are the focus of this research. Here, we report and analyze the behavior of the blinking phenomena on a nanopillar sample. We noticed that the blinking of the pillars is somehow synchronized on a long timescale among several spatially separated nanopillars. We demonstrated that the synchronization is not due to random intensity fluctuations. We suggest instead that the synchronization is caused by a nonlinear response of the quantum wells to the UV source. In other words, when the stimulation intensity surpasses a certain value, it triggers an ON/OFF state switch in the PL of some of the pillars. Even if preliminary, our study helps to provide clues to understanding the mechanism of the occurrence of the blink phenomenon.

Radiation-photon converter based on GaN single crystal coupled with multi-quantum-well luminescence structure

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Converting radiation into optical signals is a fundamental method for nuclear radiation detection. However, traditional scintillators encounter a trade-off between efficiency and response speed. This research proposes a radiation-photon converter constructed from multi-quantum-well (MQW) structures integrated into radiation-sensitive materials, providing a unique solution to this challenge. The prototype was fabricated using a homogeneous epitaxial layer of GaN on a semi-insulating substrate. The radiation-photon conversion process was facilitated by directing charge carriers generated from radiation energy deposited in the semi-insulating substrate to the MQW layer via an external electric field. The converter exhibited a sensitive and rapid response to x-ray irradiation, enabling modulation of the excited photon wavelength through the MQW layers. Luminescence spectrum tests demonstrated that the net luminescence intensity increased with rising device voltage. Imaging experiments revealed that the grayscale values of device photographs, under the combined influence of electric fields and x rays, correlated with the trend in net current variation. These findings confirmed the effective conversion of radiation into optical signals through the modulation mechanism of the electric field, highlighting significant implications for the

development of advanced radiation detection methodologies.

Efficiency droop of AlGaN-based deep-ultraviolet miniaturized light-emitting diodes under electrical stress

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The reduction on efficiency of AlGaN-based high-voltage (HV) deep ultraviolet light emitting diodes (DUV-LEDs) with quadra-serial connection and different geometries has been investigated under electrical stress. After the electrical aging, the Shockley–Read–Hall nonradiative recombination becomes more significant, while the Auger recombination is mitigated. The hexagonal HV DUV-LEDs reach a maximum external quantum efficiency of 6.1% and exhibit superior performance after aging. The results provide insights into the impacts of submesa geometry on reliability and UV light communication performance of HV DUV-LEDs.

Manipulating precursors of group-III nitrides for high-Al-content p-AlGaN toward efficient deep ultraviolet light emitters

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The high-Al-content p-AlGaN electron blocking layer (EBL) is essential for mitigating electron overflow in deep ultraviolet light-emitting diodes (DUV LEDs) but suffers from poor conductivity. One of the reasons is that the carbon impurity may act as donor-like compensating defect, which is incorporated into the epilayers by the metalorganic chemical vapor deposition. To grow the high-Al-content p-EBL and minimize carbon incorporation, we proposed a group-III nitrides precursor modulation strategy. This technique involves reducing the flow rates of metalorganic precursors, trimethylaluminum, and trimethylindium, while maintaining the Al/Ga ratio. By this method, the p-Al0.8Ga0.2N EBL with an ultralow carbon concentration of 1016 cm−3 was grown. Moreover, the high initial composition in the EBL leads to a larger compositional gradient in the adjacent p-AlGaN graded layer, which increases bulk polarization-induced hole concentration compared with the p-Al0.7Ga03N EBL. Together, these factors above contribute to a 20% enhancement in light output power and a 6% reduction in operation voltage at 40 mA in the proposed DUV LED statistically. This feasible growth scheme provides a promising strategy for the high-efficiency and cost-competitive DUV LEDs.

Removal of hydrogen by electric and polarized fields for high-performance AlGaN deep-ultraviolet-C light emitting diodes

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The dehydrogenation of the Mg–H complex to increase the hole concentration is crucial for promoting the performance of ultraviolet-C light-emitting diodes (UVC-LEDs). Here, we systematically investigate the efficient removal of H atoms through combining external electric field produced by electrochemical process and polarized electric field of p-AlGaN. The measured electroluminescence spectra show the emission intensity of optimized AlGaN structure achieving a large increment of 12.5% after the H removal. Furthermore, the reliability and lifetime of UVC-LEDs are also significantly promoted by our methods. The physical mechanism of the coupling interaction between external and polarized electric fields on H removal is further elucidated through the

first-principles calculations. The density of states, electrostatic potential energies, and differential charge densities of Mg–H doping AlGaN under various electric fields reveal that the charge redistributions and huge electrostatic potential difference between Mg and H atoms are responsible for the breaking of Mg–H bonds and expelling of H atoms. This work offers feasible strategy to promote the applications of AlGaN-based UVC-LEDs.

Investigation of InGaN-based flexible RGB micro-light-emitting diodes and their monolithic integration

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This study demonstrated InGaN-based flexible RGB micro-light-emitting diodes (µLEDs) with size ranging from 20 to 100 µm through laser liftoff and UV-tape-assisted transfer process. The fabrication process of flexible RGB µLEDs released the stress of GaN films, which reduced the bending of energy band and screened the quantum-confined Stark effect in InGaN quantum wells based on theoretical simulation. Thus, a clear blue shift of peak wavelength was observed especially for red µLEDs. The electrical and electroluminescent performance, such as forward voltage, peak wavelength, and full width half maximum of flexible RGB µLEDs, could remain approximately identical under different bending radii from 3 to 7 mm. We realized the monolithic integration of flexible RGB µLEDs and obtained a wide color gamut that covered around 78% of the Rec. 2020 at bending conditions.

Temperature-Induced Stress Performance of High-Density GaN Micro-LED Arrays for Industrial Mass Production

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The high-temperature-induced stress performance of GaN-based blue micro light emitting-diode (micro-LED) arrays with a pixel size of 5 × 5 µm2 (6 µm pitch) is studied, and monochrome micro-LED displays with 4233 PPI for industrial mass production are demonstrated. The temperature-induced stress performance of the micro-LED arrays with the same pixel size is evaluated under identical measurement conditions as a function of the temperature to observe the changes in optoelectronic performance before and after temperature-dependent electroluminescence (TDEL) measurements. The photoluminescence (PL) intensities of each pixel in a matrix (2 × 2 pixels) for site 1 (center), site 2 (near sidewall), and site 3 (sidewall) decreased after TDEL measurement, and the reduction rates of peak wavelength intensity at site 1, site 2, and site 3 are 31.37%, 62.95%, and 65.11%, respectively. In addition, the light distribution of the two pixels on the right is degraded after TDEL measurement because high-temperature measurement creates point defects at mesa-sidewalls that act as nonradiative recombination centers. However, the forward voltage (VF) variations for a single pixel and for 120 pixels in five different regions on a 4 in. wafer are only 0.02 V

(0.72%) and 0.04 V (1.42%), respectively. The zoomed-in image of the passive matrix-type blue micro-LED arrays showing light emittance demonstrates good display uniformity and brightness simultaneously at 1710 pixels. The obtained results have important implications for the advancement and potential commercial viability of micro-LED displays, demonstrating their ability to meet stringent image quality standards in real-world applications.

Multifunctional III-nitride optoelectronic system on a tiny chip

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AIP Advances
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Multi-quantum well (MQW) diodes exhibit simultaneous emission and detection, allowing them to serve as multifunctional devices, including light emitters, receivers, energy transmitters, and information transmitters. Leveraging this capability, we designed a Multifunctional Energy Transfer Information System (METIS) that integrates contactless control, energy harvesting, and information transfer. At the core of this system, the multifunctional energy communication chip operates effectively across a broad range of extreme temperatures and in various solution environments. As the ambient temperature varies from −60 to 120 °C, the peak emission wavelength shifts from 465 to 476 nm, and even with further temperature changes from −70 to 150 °C, the communication function remains stable. Encapsulated for durability, METIS functions reliably in extreme conditions such as ice, water, salt solutions, and other light-transmitting fluids without needing external circuitry. Additionally, we demonstrate passive control of analog switches via MQW diodes. The MQW diodes also enable contactless energy and optical information transfer, ensuring stable and controllable information reconstruction at the receiving end. This approach offers an innovative solution for energy and information transmission in extreme environments.

The transmission modulation effect of patterns on the light extraction of ultraviolet-C light emitting diodes

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The AlGaN-based ultraviolet-C light emitting diodes (UVC LEDs) exhibit low light extraction efficiency (LEE), and patterning substrate surfaces is considered an effective solution. In this work, a simplified model based on the light extraction process of typical flip-chip UVC LEDs is proposed, which accelerates the simulations and illustrates the transmission process of patterned substrates more clearly. It is found that, different from the case in InGaN-based visible LEDs, the patterns on the substrate surfaces of UVC LEDs enhance the LEE by modulating the transmittance. The effects of sub-micron patterns are also studied, and the results suggest that the effects of LEE enhancement from different-scaled patterns vary little, unless the scale is decreased below a certain threshold so that the LEE decreases significantly. The results also show that AlN substrates can exhibit a 33% relative LEE enhancement if properly patterned, in contrast to the 18% enhancement in the case of sapphire. The proposed models and the acquired conclusions should be of help in designing UVC LEDs with high efficiency, especially for those on AlN substrates.

Development of all-solid-state ultraviolet lasers

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Since the discovery of the frequency doubling phenomenon in the 1960s, there has been a continuous emergence of solid-state lasers with

varying wavelengths. Technological advancements have facilitated the generation of various types of ultraviolet lasers by employing diverse frequency doubling crystals and pump sources. Ultraviolet lasers find widespread applications in processing, microelectronics, grating fabrication, and beyond. This article presents a comparative analysis of the strengths and weaknesses of different ultraviolet lasers, explores solid-state ultraviolet lasers of varying wavelengths achieved through frequency doubling, and delineates their diverse applications.

Insight into gain and transient response characteristics of AlGaN/GaN hetero-junction based UV photodetectors: Case study on the role of incident light intensity

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Gain and response speed are two key performance parameters for high sensitivity photodetectors (PDs). However, the effect of incident light intensity on gain and transient response properties of AlGaN/GaN hetero-junction based PDs are still not fully understood. Here, we design and fabricate an AlGaN/GaN hetero-junction based ultraviolet (UV) PD with interdigitated electrodes formed by a conductive two-dimensional electron gas (2DEG) channel, which exhibits a low dark current of $2.92 \times 10{-}11$ A and a high responsivity of 3060 A/W at 10 V bias. The high-gain AlGaN/GaN 2DEG PD has a similar working mechanism to those of traditional phototransistors, but its device architecture is evidently simplified. By investigating the variation of gain and transient response characteristics of the 2DEG PD as a function of incident UV light intensity, it has been concluded that the gain of the PD in a low-light intensity region is dominated by hole accumulation-induced electron escape from the 2DEG, while in a high-light intensity region, the gain is dominated by photoconductivity effect and limited by carrier recombination. This study provides guidance for future practical applications of AlGaN/GaN-based PDs in complex UV illumination environments.

A Review of Challenges, Solutions, and Improvements in the Performance of Deep Ultraviolet Semiconductor Laser Diodes (DUV LDs)

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As eco-friendly light sources, AlGaN-based deep ultraviolet laser diodes (AlGaN DUV LDs) employing aluminum gallium nitride that emit between 200 and 300 nm have seen various applications in replacing the traditional mercury DUV light sources, such as photolithography, fluorescence microscopy, and water purification. In this review, we present structures, applications, and advantages of the AlGaN DUV LDs. In addition, limitations and challenges of the AlGaN DUV LDs will be covered. A comparative analysis of the previous researchers' work regarding strategies that include various designs of electron blocking layers (EBLs), cladding layers, waveguides, and quantum barriers in enhancing the performance of DUV LDs will be reviewed, and the underlying physics of these designs in improving the performance of AlGaN DUV LDs will be discussed.

Visible-Telecom Entangled-Photon Pair Generation with Integrated Photonics: Guidelines and a Materials Comparison

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Correlated photon-pair sources are key components for quantum computing, networking, synchronization, and sensing applications. Integrated photonics has enabled chip-scale sources using nonlinear processes, producing high-rate time–energy and polarization entanglement at telecom wavelengths with sub-100 microwatt pump power. Many quantum systems operate in the visible or near-infrared ranges, necessitating visible-telecom entangled-pair sources for connecting remote systems via entanglement swapping and teleportation. This study evaluates biphoton pair generation and time–energy entanglement through spontaneous four-wave mixing in various nonlinear integrated photonic materials, including silicon nitride, lithium niobate, aluminum gallium arsenide, indium gallium phosphide, and gallium nitride. We demonstrate how geometric dispersion engineering facilitates phase-matching for each platform and reveals unexpected results, such as robust designs to fabrication variations and a Type-1 cross-polarized phase-matching condition for III–V materials that expands the operational wavelength range.

Mechanism of Indium Redistribution and Thermal Degradation in InGaN/(In)GaN Quantum Wells of Vertical Cavity Surface Emitting Lasers

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The redistribution and segregation behavior of indium atoms in InGaN multiple quantum wells (MQWs) have been observed during the thermal annealing process in a vertical cavity surface emitting laser (VCSEL) structure. The migration of indium atoms may lead to a thermal degradation of InGaN/(In)GaN MQWs, resulting in the decomposition of InGaN QW and quantum barrier (QB) layers as well as the broadening of QW layers. Photoluminescence (PL) mapping measurements indicate that indium aggregation occurs in QWs without protection, which will cause the inhomogeneous luminescence of the MQW and decrease the laser optical performance. Temperature-dependent and excitation power-dependent PL spectra were employed to examine the presence of nonradiative recombination centers in deep localized states formed by indium aggregation, which also deteriorate the luminescence performance. Furthermore, a protective structure containing an InGaN or GaN sacrifice layer is proposed to suppress thermal degradation and improve the luminescence performance.

ELECTRONICS

A 2DEG-Based GaN-on-Si Terahertz Modulator with Multi-Mode Switchable Control

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Advanced Optical Materials
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As terahertz (THz) technology has been widely considered as a key candidate for future sixth-generation wireless communication networks, THz modulators show profound significance in wireless communication, data storage, and imaging. In special, dynamic tuning of THz waves through 2D electron gas (2DEG) incorporated with a hybrid design of metasurface has attracted keen interest due to the combined merits of deliberate structural design, rapid switching speed and the process compatibility. Current meta-modulator enables very high modulation depth but encounter limited bandwidth. In this paper, by taking into account the co-functional effects of temperature and voltage-dependent dynamic control on transmission amplitude, a 2DEG-based GaN-on-Si modulator with two switchable operational states (or four modes) of active wave control is proposed. Under cryogenic temperature conditions, the proposed device exhibits prominent 2D plasmons characteristics with switchable transitions between the gated mode and ungated mode for active control. Under room temperature conditions, the proposed device exhibits non-resonance broadband spectra characteristics with tunable transitions between the linearity mode and depletion mode for transmission control. The scheme provides an option for the development of the actively tunable THz meta-modulator and paves a way for the robust multifunctionality of electrically controllable THz switching, and biosensors.

Sensitive Microwave Rectifier for High-Power Wireless Transfer Based on Ultra-Low Turn-On Voltage Quasi-Vertical GaN SBD

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This paper presents the theoretical analysis and experimental validation of a harmonic-terminated high-efficiency and high-power microwave rectifier. The rectifier is designed utilizing a single-circuit gallium nitride (GaN) quasi-vertical Schottky barrier diode (SBD). Capitalizing on the strengths of wide bandgap, high mobility and high saturation velocity of the GaN, the SBD achieved a high breakdown voltage of 180 V and an ultra-low turn-on voltage of 0.23 V (at 1 A/cm 2). These characteristics enhance rectification performance across both high and low input power regions, making it suitable for wireless power transfer (WPT) applications. The optimized high-power microwave rectifier incorporates this advanced diode, featuring a wide input power range and high efficiency. The proposed rectifier structure includes a single-shunt self-developed SBD and topology with a harmonics compression network. It accomplishes a maximum RF-to-DC power conversion efficiency of 70.4% with an input power of 42 dBm (15.8 W) at 0.9 GHz. The highest efficient power handling ability is up to 20 W with an 18 dB (25–43 dBm) dynamic range achieving an efficiency exceeding 50%, demonstrating the high potential of high-power GaN SBDs for wireless high-power transfer for future microwave WPT applications.

Recent Developments, Reliability Issues, Challenges and Applications of GaN HEMT Technology

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IEEE Electron Devices Reviews
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The increasing demand for high-power and high-frequency electronics has led to the development of new materials and devices. One such material is gallium nitride (GaN), which has superior properties for power and radio frequency (RF) applications. This review paper covers various aspects of GaN HEMTs, including the early developments. The paper also presents state-of-the-art techniques that provide further insight into these devices. In addition, the review identifies some of the reliability issues and challenges that need to be addressed in order to realize the full potential of the devices. Moreover, the practical applications of GaN HEMTs across various domains are mentioned. These applications span telecommunications, where they are integral components in high-power amplifiers for base stations, to radar systems, where their high-frequency performance enables precise signal detection. Moreover, they find utility in satellite communication systems, facilitating efficient power amplification and signal processing.

A 4.5–5.5-GHz Compact 6-bit Phase Shifter with Low RMS Phase and Amplitude Errors Based on Bandpass Structure for High-Power Applications

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This article presents a compact 6-bit digital phase shifter (PS) monolithic microwave integrated circuit (MMIC) with low root-mean-square (rms) phase and amplitude errors. A novel bandpass phase-shifting cell (PSC) with embedded high-isolation switches is proposed and adopted in 180 ∘ -and 90 ∘ -bit designs to compensate the isolation-degradation caused by the large drain–source capacitance of GaN transistors. Then, a systematic design method is investigated to minimize phase and amplitude errors. To validate the proposed techniques, a 6-bit C -band PS is implemented in a 0.25 μ m GaN-on-SiC HEMT process with a circuit size of 1.9 × 2.5 mm 2 (0.03 × 0.04 λ2). The measured rms phase error of the proposed PS is less than 1.2 ∘ from 4.5 to 5.5 GHz with a 2.8 ∘ calibration bit. The insertion loss (IL) varies between 5.8 and 8.2 dB with an rms amplitude error of less than 0.5 dB. Besides, a good power linearity with 37.9 dBm input 1 dB compression point (IP 1dB) and 49.8 dBm input third-order output-referred intercept point (IIP3) is also attained. The proposed PS exhibits superb overall performances in phase resolution, phase/amplitude error control, IL, and power handling capability within a small chip size. It can be a potential candidate for various systems including radars, cellular base stations, and avionic devices.

Diagnosing Thermal-Interface Aging of Power Devices using Self-Sensing

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IEEE Transactions on Power Electronics
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This paper proposes a unique and simple method that diagnoses multiple aging effects in power electronic devices minimally invasively and without the necessity of expensive sensors. Different degradation modes, e.g. fatigue of solder and thermal-interface layers, influence the phase of the thermal impedance frequency response function ∠Z—th(jω) at specific bandwidths. Thus, tracking changes of the thermal impedance's phase i.e., the phase shift between periodic device-loss excitation at specific frequencies and the resulting junction temperature response allows identifying these degradation modes. This is exploited by the proposed method for degradation diagnosis which takes advantage of the temperature dependency of the drain-source voltage. The method excites periodic conduction losses at selected frequencies via small-signal manipulation of the gate-source voltage and measures the phase delay between gate-source and drain-source voltage. The measurable phase delay results partially from the dynamic response of the thermal impedance, because the

phase-delayed junction temperature impacts the on-state resistance and therefore the drain-source voltage. Consequently, changes of the measurable phase delay allow identifying changes of ∠Z—th(jω) and thus diagnosing the above mentioned degradation modes. The paper features a detailed analysis of the proposed method using a general sensitivity analysis. A detailed analysis shows that the discussed method is applicable for silicon (Si) MOSFETs, gallium nitride (GaN) HEMTs as well as silicon carbide (SiC) MOSFETs. Experiments with SiC MOSFETs, being the most emerging technology in industry, demonstrate that the implemented method can effectively diagnose changes of the thermal path between the device and the heat sink that result from different degradation modes.

Augmented Phase-Normalized Recurrent Neural Network for RF Power Amplifier Linearization

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IEEE Transactions on Microwave Theory and Techniques
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In this article, we present a highly accurate recurrent neural network (RNN) for behavioral modeling and digital predistortion (DPD) of radio frequency (RF) power amplifiers (PAs). We describe a deep, residual recurrent unit (RRU) that minimizes the overhead of the recurrent operation. Phase normalization is incorporated with the proposed unit to allow for efficient processing of the baseband signal phase with the real-valued RNN structure. Furthermore, we augment the phase normalization concept with dedicated envelope cell states that support the mapping of RF envelope dominated distortions. Combination with a trainable, input-ended finite impulse response (FIR) filtering leads us to proposing the augmented phase-normalized RRU (APNRRU). Our experimental validation, including a detailed modeling study of the proposed concepts with three different GaN Doherty PA units, as well as several DPD linearization examples, shows that the APNRRU offers excellent linearization already with modest complexity of just 550 model parameters. In addition, the results demonstrate the ability to linearize also demanding wideband PA operation with noncontiguous multicarrier signals with 400-MHz composite bandwidth, outperforming the prior art solutions.

K/Ka-Band–GaN–HEMT with 700 mS mm^{-1} Extrinsic Transconductance

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physica status solidi a
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In this study, the impacts of fabrication technology and epitaxial layer design on the transconductance (gm) of radio frequency AlGaN/GaN high-electron-mobility transistors (HEMTs) are examined. Optimization of the SiNx passivation and AlGaN barrier design of 150 nm gate HEMTs enhances the extrinsic (at Vds = 10 V) and intrinsic (at Vds = 15 V) transconductance from ≈0.47/0.65 to ≈0.62/1.1 S mm−1. Notably, an extrinsic gm of 0.70 S mm−1 at Vds = 5 V is achieved, setting a new benchmark for the extrinsic transconductance of AlGaN/GaN HEMTs designed for the K/Ka frequency range with a breakdown voltage exceeding 100 V.

Low Contact Resistivity of < 10Ω· mm for Au-Free Ohmic Contact on p-GaN/AlGaN/GaN

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A robust Au-free p-type ohmic contact process with ultralow contact resistivity is developed on p-GaN/AlGaN/GaN, which demonstrates the potential of GaN CMOS to be compatible with Si CMOS process lines. A novel metal stack of Mg/Ni/Pt is designed, and ultralow contact resistivity of 8 Ω·mm (1.0×10 -5 Ω·cm2) is achieved. It is revealed that the Ga vacancies

on the p-GaN surface induced by Ni, and the Ni 2 O 3 embed in the decomposed p-GaN are key to forming stable low resistivity ohmic contact.

E-mode AlN/GaN HEMTs on Si with 80.4% PAE at 3.6 GHz for Low-Supply-Voltage RF Power Applications

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IEEE Electron Device Letters
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Enhancement-mode (E-mode) AlN/GaN high electron mobility transistors (HEMTs) with a 160-nm T-shape recessed gate on a silicon substrate were fabricated. The fabricated device has a V TH of +0.35 V, and shows a maximum drain current (I DMAX) of 1.58 A/mm, a low on-resistance (R ON) of 1.8 Ω·mm, and a peak transconductance (G MMAX) over 580 mS/mm. A cut-off frequency (f T) of 85 GHz and a maximum oscillation frequency (f max) of 75 GHz were obtained. Load pull continuous-wave (CW) power sweep measurement at 3.6 GHz demonstrated a peak power-added-efficiency (PAE) of 71.4% and a saturated output power density (P out) of 0.70 W/mm at V DS = 6 V. At 3.6 GHz pulsed wave (PW) power sweep at V DS = 6 V the device demonstrated an 80.4% PAE and 0.5 W/mm associated P out . These results promises the great potential of E-mode AlN/GaN HEMTs with gate recess in the applications of low supply voltage RF power applications.

A Broadband and Transient-Accurate AlGaN/GaN HEMT SPICE Model for X-Band RF Applications

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Dispersive effects such as trapping play a vital role in determining the performance of AlGaN/gallium nitride (GaN) high-electron mobility transistors (HEMTs) for RF and power applications—necessitating accurate modeling for robust circuit designs. This work presents a rigorous SPICE model to capture the transient and large-signal impact of traps in AlGaN/GaN HEMTs. The model has been implemented in the industry-standard ASM-HEMT compact-model framework. The model accurately accounts for the variation in threshold voltage and change in 2DEG charge carrier concentration in the source- and drain-side access regions under various drain-lag and gate-lag quiescent conditions. Threshold voltage and 2DEG charge carrier concentration at the source- and drain-side access regions show a linear dependence on drain-lag and gate-lag quiescent conditions, respectively. The results obtained using the developed model are in good agreement with the measured data. This model is valid for transient current simulations at different quiescent conditions and accurately captures the large-signal behavior at the optimal load impedance. Finally, pulsed IV characteristics at different temperatures have been validated against device measurements.

Characterization of Drain-Induced Barrier Lowering in GaN HEMTs Using a Drain Current Injection Technique

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Assessing short channel effects (SCEs) is crucial in the high-frequency optimization of downscaled field-effect transistors (FETs) such as GaN high electron mobility transistors (HEMTs). Drain-induced barrier lowering (DIBL) is commonly used for quantifying the ability of the gate to modulate the drain-source current at high drain voltages. DIBL is traditionally extracted from the relative shift of the threshold voltage at different drain-source voltages. In this article, we propose a new method based on a drain current injection technique (DCIT) to assess DIBL. This method facilitates a direct measure of the threshold voltage over a wide range of drain-source voltages in a single measurement. The method is demonstrated and compared to the conventional method using

AlGaN/GaN and InAlGaN HEMTs with a Fe-doped buffer and a C-doped AlGaN back-barrier, respectively. Furthermore, the impact of different gate lengths and GaN channel layer thicknesses is presented. The measurements are analyzed and discussed with supporting technology computer-aided design (TCAD) simulations. The proposed method facilitates a more general and detailed measurement of the DIBL for HEMTs.

Microwave and Millimeter-Wave GaN and GaAs ICs: High performance from 1 to 100 GHz

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IEEE Solid-State Circuits Magazine
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This paper presents an overview of microwave and millimeter-wave III-V semiconductor circuits designed by graduate students as a part of their training. The monolithic microwave integrated circuits (MMICs) are designed for a wide range of applications, ranging from an on-chip GaAs Dicke radiometer at 1.4 GHz for non-invasive internal body temperature measurements, to a transmit-receive GaN chip from 75-110 GHz with about 1W of maximum output power and a minimum noise figure of 4.2 dB in transmit and receive mode, respectively. Several other circuits are briefly discussed, e.g. high-efficiency transmitters for high peak-to-average ratio (PAPR) signals and rectifying arrays for wireless power reception.

Trap Location and Stress Degradation Analysis of GaN High Electron Mobility Transistors Based on the Transient Current Method

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IEEE Transactions on Device and Materials Reliability
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In this paper, the carrier trapping behavior and electrical characteristics of AlGaN/GaN high electron mobility transistors (HEMTs) under different bias conditions are studied based on the transient current. By considering the transient drain current of HEMTs at different temperatures, three trapping mechanisms are identified: (1) charge trapping in the AlGaN barrier layer, in the gate-drain region near the two-dimensional electron gas (2DEG) channel; (2) charge trapping in the GaN layer, in the gate-drain region near the gate; and (3) charge trapping on the surface of the AlGaN layer, in the gate-drain region near the gate. The influences of the source-gate and drain-gate voltages on trapping behavior are analyzed to further elucidate the trap locations. The experimental results show that charge capture is mainly affected by the drain-gate voltage. High electric field stress affects the local structure order inside the device, thus affecting the charge escape rate. The threshold voltage shift is mainly affected by the surface trap of the AlGaN layer near the gate.

Monolithic Integrated Micro-Thin-Film Thermocouples for On-Chip Temperature Measurement of GaN HEMTs

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IEEE Transactions on Electron Devices
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Gallium nitride (GaN) is crucial in power devices due to its wide bandgap, high electron mobility, and high critical field. GaN devices, such as high electron mobility transistors (HEMTs), are vital for high-power and high-frequency applications and can withstand high temperatures. However, these devices could encounter self-heating effects at high power, causing current collapse and performance degradation. The accurate temperature monitoring in GaN devices is essential for maintaining performance and avoiding failures. Micro-thin-film thermocouples (micro-TFTCs) offer a solution with their high-resolution and direct temperature measurements. These thermocouples, integrated onto device surfaces, bypass the limitations of other methods. In this work, we demonstrate the monolithic integration of micro-TFTCs into GaN HEMTs, using a platinum-chromium junction with a sensitivity of 19.23 ± 0.405 μ V/°C. This enabled precise monitoring of GaN HEMT channel (channel width =200 μ m) temperatures, with a measured temperature of 68.54 ◦ C ± 0.16 ◦ C at a power density of 5.72 W/mm, highlighting the effectiveness of this technique in thermal characterization of semiconductor devices.

Direct Drive D-Mode GaN HEMT Switching Characteristics and Turn-off Loss Reductions

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IEEE Transactions on Power Electronics
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This paper aims to evaluate the depletion-mode gallium nitride high electron mobility transistor (d-mode GaN HEMT) using direct-drive gating and double-pulse-test (DPT) to assess switching energy. The gate driving circuit features a modified cascode structure for 'normally off' operation and a charge-pump circuit to supply a negative gate voltage for turn-off operation. This paper described these features theoretically and validated with experimental results. Similar to enhancement-mode (e-mode) power MOSFETs or HEMTs, adjusting the gate drive resistance can affect the switching speed and associated losses, but the d-mode GaN HEMTs present an additional feature with turn-off loss reduction through gate voltage control. Thus, the main contribution of this paper is to propose and demonstrate significant turn-off loss reduction using the direct-drive approach for d-mode GaN HEMTs.

A 360 ∘ Tunable Phase Shifter with Low Phase Error Based on Bandpass Networks in 0.25- μ m GaN Technology

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IEEE Transactions on Very Large Scale Integration (VLSI) Systems
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This brief presents a 360 ∘ tunable phase shifter (PS) with low phase error in a 0.25- μ m GaN-on-SiC HEMT process. To achieve these features, the design incorporates two key innovations: a novel switched-bandpass phase-shifting cell (PSC) topology and a Q -learning-based optimization algorithm, both applied for the first time in monolithic microwave integrated circuit (MMIC) PS designs. The adverse effects of the charge trapping effect in GaN HEMT switches are mitigated by using a nonlinear equivalent circuit model. A PS prototype consisting of a fifth-order bandpass PSC and two third-order bandpass PSCs with a core area of 1.25 × 2.5 mm 2 is designed, fabricated, and measured. Experimental results demonstrate a low rms phase error of less than 7.0 ∘ , along with high power linearity characterized by an IP 1 dB of 37 dBm and an IIP3 of 48 dBm, over a frequency range from 4.1 to 5.3 GHz.

Monolithically Integrated Bidirectional Gate ESD Protection Scheme of p-GaN Power HEMT by Dual-Gate Device Technology

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IEEE Transactions on Power Electronics
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This letter proposes a monolithically integrated bidirectional gate electrostatic discharge protection scheme for p-GaN power high-electron-mobility transistors (HEMTs), in which a dual-gate HEMT is designed as the discharging transistor. With this protection scheme, the forward/reverse transmission line pulsing failure current is enhanced from 0.156 A/0.08 A to 1.36 A/5.26 A, almost without sacrificing performances of the p-GaN power HEMT. Thanks to the bidirectional switching characteristics of the dual-gate device by sharing the drift region, only one discharging transistor is required in the scheme; as a result, the area of this protection scheme can be effectively saved by 40.8% compared to state-of-the-art scheme with the same protection capability.

Numerical Analysis for Negative Discharge Under High-Frequency Pulsed Voltage

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IEEE Transactions on Magnetics
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The increase in renewable energy and the development of Silicon Carbide (SiC) and Gallium

Nitride (GaN) power switches have led to higher voltage magnitudes, slew rates, and switching frequencies, imposing greater electric stress on insulating materials. However, it is hard to recognize the partial discharge signal from background noise due to electromagnetic interference when diagnosing electrical equipment with high switching frequency. Therefore, we numerically analyzed negative corona discharge under a superposition of direct current (DC) and pulse-width modulation (PWM) voltage, with a switching frequency of 80 kHz in a needle-plane geometry varying rising times of 100, 200, and 500 ns. The analysis model was coupled with Poisson's equation and the drift-diffusion model. We considered three types of charge carriers—electrons, positive ions, and negative ions—and the generation and loss of each charge carrier. The discharge current was calculated from Poynting's theorem. The discharge current pulses were regularly sustained, like the Trichel pulses in the previous research. However, the periods between pulses and the magnitude of the pulses changed depending on the applied voltage and rising time. With the increase in rising time, both the current pulse peak value and the pulse period decreased, affecting the charge distribution, especially for the ionization region and negative ions.

Design and Analysis of a Coupled-Line-Based Load-Modulated Balanced Amplifier MMIC With Enhanced Bandwidth Performance

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IEEE Transactions on Circuits and Systems I: Regular Papers
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This article presents the design theory and implementation of a fully integrated coupled-line-based load-modulated balanced amplifier (CLLMBA) monolithic microwave integrated circuit (MMIC). To facilitate the design, a novel design method is proposed for the CLLMBA to precisely control the load modulation and output power back-off (OBO) level by arranging the current ratio among the control amplifier (CA) and balanced amplifiers (BAs). Moreover, to further expand the working bandwidth, the coupled-line couplers are adopted in the CLLMBA. Subsequently, the physical dimensions and operating conditions of the three sub-amplifiers are selected accurately based on load modulation analysis at the fundamental frequency. It leads to properly modulated impedances and cancels the output matching networks for sub-amplifiers. Besides, meandering lange couplers are adopted by double metal layers and air-bridges for a compact layout. To validate the proposed techniques, a CLLMBA prototype is implemented and fabricated in a commercial 0.25- μ m GaN HEMT process with the die size of 3.1×2.3 mm 2 . The measurement result exhibits a 38.1-39.3 dBm saturated output power with a 45.8%-57.6% saturated drain efficiency (DE), and a 31.7%-42.3% DE at 10-dB OBO from 4 to 6 GHz. Furthermore, under a 100 MHz orthogonal frequency division multiplexing (OFDM) signal with 8.5 dB peak-to-average power ratio (PAPR), the average DE is 32.8%-40.6% and the adjacent channel leakage ratio (ACLR) after digital predistortion is better than − 47.5 dBc.

An Isolated Gate Driver Enabled by Simultaneous Wireless Information and Power Transfer

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IEEE Transactions on Microwave Theory and Techniques
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Wide-bandgap semiconductor devices, such as gallium nitride (GaN) or silicon carbide (SiC), are key enablers for innovative power electronic circuit topologies. However, novel types of isolated gate drivers with high common-mode transient immunity (CMTI) and high switching speed need to be developed to put these benefits into action. We propose a radio frequency gate driver (RFGD), which utilizes a single radio frequency coupling channel and simultaneous wireless information and power transfer (SWIPT) at a 2.4-GHz carrier frequency and harmonic backscattering for monitoring signal transmission. A hybrid prototype is implemented, and the measurements are

demonstrated. The prototype components are validated individually, and the full system is showcased by driving the gate of an eGaN-FET in a common-drain circuit. The transferred switching signal is pulsewidth modulated (PWM) at 62.5 kHz and modulates a 2.6-kHz sine wave. The prototype draws its entire power from a single 282-mW RF input signal at this operating point. The CMTI RFGD of the prototype is discussed and related to the signal-to-noise ratio (SNR) of the receiver path.

Design and Validation of a Cost-Effective 300 W GaN-Based Step-Up Push-Pull Converter

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The integration of Wide Bandgap (WBG) semiconductors has enhanced the performance of switching power supplies in terms of both efficiency and power density. However, the fast-switching dynamics of these devices, particularly in Gallium Nitride (GaN) semiconductors, amplify the impact of parasitic elements in the circuit, demanding new methods and tools in power converter design. To address this problem, a multi-objective design method for a GaN-based isolated DC-DC converter is presented, complemented by an analytical Double Pulse Test (DPT) model. This method is applied to select the optimal components and switching frequency for a push-pull converter, resulting in the design of a GaN-based step-up DC-DC converter. The analytical estimations for power losses and overvoltage are validated through a GaN-based push-pull prototype. The design achieves an efficiency of 93% under nominal conditions, with a power density of 2.23 W/cm3, and a total component cost of 17.5 € for the magnetics, capacitors, and semiconductors. This approach not only demonstrates significant improvement in terms of efficiency, volume, and cost compared to silicon-based isolated DC-DC converters but also offers a promising design methodology to improve isolated DC-DC converters in modern power conversion applications.

A GaN-on-SiC Millimeter-Wave Low Noise Amplifier Using Hybrid-Matching Technique for 5G n258 Applications

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Microwave and optical technology letters
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This letter details the design and implementation of a millimeter-wave (mm-Wave) low noise amplifier (LNA) employing 150-nm gallium nitride on silicon carbide (GaN-on-SiC) high electron mobility transistor technology, specifically tailored for fifth-generation (5G) applications. The proposed GaN-based LNA integrates a hybrid matching topology alongside a co-design strategy, thereby optimizing the noise figure (NF) by minimizing interstage matching components. The fabricated LNA, spanning a total chip area of $2.3 \times 1.4\ mm^2$, exhibits a linear gain in the range of 17.41–19.2 dB and maintains an NF within 2.32–3.06 dB. Additionally, commendable input/output return losses exceeding 7.5 dB are achieved across the 23–27.5 GHz, with the apparatus consuming approximately 150 mW.

A High Power Density Ku-Band GaN Power Amplifier Based on Device-Level Thermal Analysis

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International Journal of Numerical Modelling
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This paper introduces a new design method for a high-power density GaN MMIC amplifier operating in the Ku-band. A thermal model to investigate the thermal distribution of power amplifiers is proposed to achieve optimal performance in terms of power density, chip size, and channel temperature. The thermal distribution and channel temperature of a single device, an eight-way parallel device combination, and the entire PA layout are obtained by finite element simulation. The thermal coupling effects of high-power MMICs are analyzed in detail. The thermal resistances are extracted from the simulation to design a Ku-band

amplifier. Measurement results demonstrate that the designed amplifier achieves 43.0–44.2 dBm output power and 22.7%–34.5% PAE at 28 V drain voltage with a 100 µs pulse width and 10% duty cycle within 12–18 GHz. The proposed design method enables the amplifier to have a compact layout of 10.88 mm2 and a power density between 1.84 and 2.42 W/mm. This design method can offer valuable insights for future development of high-power MMIC amplifiers.

Au-Free Ti/Al/Ni/TiN Ohmic Contact to AlGaN/GaN Heterostructure: Ti/Al Thicknesses at an Optimized Ratio

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Although a few studies report that tuning Ti/Al thicknesses at a fixed ratio can further improve the Ohmic contact to AlGaN/GaN heterostructure, systematic physical mechanisms have not been reported. In this work, after determining the optimal Ti/Al ratio of 1/4, two metal stacks with varying Ti/Al thicknesses and fixed Ni/TiN thicknesses are deposited to investigate how tuning Ti/Al thicknesses at an optimized ratio enhances the Ohmic contact performance. At the optimal annealing condition (950 °C, 45 s) of samples with Ti/Al thicknesses of 20/80 nm, samples with Ti/Al thicknesses of 35/140 nm exhibit a reduction of 48% in contact resistance and 70% in specific contact resistivity (ρc). By correlating the results from ρc–T measurements, time-of-flight secondary ion mass spectrometry, and high-resolution X-ray diffraction, it has been determined that this method effectively enables N-vacancies doping into the heterostructure, thereby increasing the carrier concentration and reducing both the height and width of the interfacial potential barrier, achieving a more efficient carrier transport. By avoiding the use of Au with high solubility and ductility, this approach significantly improves contact performance without adversely affecting the electrode surface morphology, demonstrating good adaptability for optimizing Au-free Ohmic contacts.

Modeling the Impact of Mg Out-Diffusion on Threshold Voltage of p-GaN/AlGaN/GaN HEMT

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IEEE Transactions on Electron Devices
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This article presents a novel analytical model for the threshold voltage (VT) of p-GaN/AlGaN/GaN high-electron-mobility transistors (HEMTs), taking into account the influence of magnesium (Mg)-dopant out-diffusion from the top p-GaN layer into the AlGaN barrier and GaN layer. The proposed model incorporates realistic Mg out-diffusion profiles to accurately estimate VT of these normally off devices. Rigorous validation of the analytical model is conducted using experimental data and well-calibrated TCAD simulations, covering a wide range of device parameters and Mg out-diffusion profiles. Furthermore, the model enables the assessment of individual contributions of Mg dopants in the AlGaN and unintentionally doped (UID)-GaN layers. It also facilitates the estimation of the effects of growth duration and temperature of the p-GaN layer on the device's threshold voltage.

High-Accuracy Thermal Resistance Measurement Method for GaN HEMTs Based on Harmonic Pulsewidth Subthreshold

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IEEE Transactions on Electron Devices
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The study on the junction temperature and thermal resistance of gallium nitride (GaN) high electron mobility transistors (HEMTs) becomes essential in order to ensure high operating reliability. Among different categories of thermal resistance measurement methods, the temperature-sensitive electrical parameter (TSEP) method exhibits unique

advantages in terms of online implementation, accuracy, and applicability. After reviewing current TSEP methods for GaN HEMTs, this article proposes a high-accuracy thermal resistance measurement method for GaN HEMTs based on a heating power modulation strategy, which is named the harmonic pulsewidth subthreshold (HPWS) method. Specifically, the sensitive linear correlation between the subthreshold swing (SS) of GaN HEMTs and temperature will be utilized, and the turn-off transients of the heating power signal will be sampled to extract the thermal resistance through frequency-domain scanning of the heating signal modulation. Thus, the proposed HPWS method can filter out negative effects caused by case temperature fluctuations and the measurement impulse signal delay, which can minimize possible errors caused by nonlinearity or low sensitivity. An experimental comparison of the proposed method with two classical methods was conducted. Main experimental comparison results of the relationship between GaN HEMT thermal resistance and drain current were also introduced. The experimental results indicated that the differences between the proposed method and two classical methods at all various drain current conditions were less than 2% . Besides, a systematic analysis was conducted on main factors determining the accuracy of the thermal resistance measurement for GaN HEMTs.

A Novel Crosstalk Suppression Method With Miller Clamp Circuit for GaN HEMTs

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IEEE Transactions on Power Electronics
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Gallium nitride (GaN) power devices exhibit noteworthy characteristics, such as high switching speeds and low conduction losses, thereby facilitating enhanced efficiency and power density in switching power converters. Nevertheless, the advantages of high switching speeds and low conduction thresholds in GaN power devices also render them susceptible to bridge-leg crosstalk. To resolve the above issue, a novel miller clamp gate driver (NMCGD) is proposed. The detailed working principles of NMCGD are firstly elucidated in this paper. In NMCGD, it utilizes the negative voltage to make the BJT in a saturated state during the shutdown process of GaN. This action effectively short-circuits a portion of the drive resistor, reducing the impedance of the drive loop and suppressing crosstalk, which also reduces gate turn-on oscillation while ensuring prompt turn-on and turn-off speeds. At the same time, the parameter design and device selection criteria are presented. Notably, this NMCGD employs a minimal number of passive components, making it suitable for integration into driver IC. Finally, the efficacy of NMCGD is validated through a double-pulse test utilizing the INN650D150A GaN HEMTs.

Minimal Switching Loss Three-Stage Active Gate Driving Strategy Based on Dynamic dv/dt Switching Model for GaN HEMT

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IEEE Transactions on Power Electronics
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The fast switching of gallium nitride high mobility transistor (GaN HEMT) results in high dv/dt and severe EMI issues, requiring a trade-off with the switching power loss. Three-stage gate drive (TSGD) can mitigate the conflict between switching speed and losses, but it is challenging to achieve minimal switching loss under the existing TSGD strategy due to the nonlinear parasitic capacitance of GaN HEMT. To address this issue, this paper proposes a minimal switching loss TSGD strategy based on a dynamic dv/dt switching model, which can achieve minimal switching loss. Firstly, based on the charge conservation principle, piecewise linear equivalent values for the parasitic capacitances of GaN HEMT are calculated. Based on the result, analytical expressions for the transient voltage and current in each switching stage are derived, which forms the dynamic dv/dt switching model and provides detailed analysis for the dv/dt nonlinearity. Furthermore, analytical expressions for switching loss during each stage are calculated,

establishing the quantitative relationship between switching loss and drive conditions. By minimizing the total loss, the required driving currents and switching timings are determined. Finally, the MSL-TSGD strategy is proposed. Experimental results demonstrate that the proposed method reduces the turn-on loss by 18.6%, and reduces the turn-on delay by 29.3%.

1200-V Fully Vertical GaN-on-Silicon p-i-n Diodes with Avalanche Capability and High On-State Current Above 10 A

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IEEE Transactions on Electron Devices
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We report on fully vertical gallium nitride (GaN)-on-silicon (Si) p-i-n diodes delivering above 1200-V soft breakdown voltage (BV). Temperature dependence measurements indicate avalanche breakdown capability reflecting the high-quality processing and epitaxy growth. The ON-state characteristics of the fabricated vertical p-i-n diodes reveal ON-resistances ranging from 0.48 m Ω· cm 2 for small anode to 1.7 m Ω· cm 2 for large anode diameters (i.e., 1 mm). The ON-state resistance increase is attributed to the thermal dissipation issues. Nevertheless, the large devices exhibit high ON-state current close to 12 A owing to an optimized process, including a deep mesa etch as edge terminations and thick Cu layer for heat sink on the backside enabled by a polyimide passivation that strengthen the mechanical robustness of the membranes. To the best of our knowledge, this represents the first demonstration of fully vertical 1200-V GaN-based devices grown on Si substrates with high-current operation above 10 A, corresponding to a Baliga figure of merit (BFOM) of 3 GW/cm 2 .

Postfault Operation of Three-Level Inverter Driven Six-Phase PMSM With Enhanced Torque Speed Region

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This paper presents an open switch postfault operational technique with enhanced torque-speed region for Three-Level (3L) Active Neutral Point Clamped (ANPC) inverter-driven Symmetrical Six-Phase (SSP) Permanent Magnet Synchronous Machines (PMSMs). Maximum Torque (MT), Minimum Loss (ML), and Single Three-Phase (STP) operations are commonly used for the postfault operations of six-phase drives. The maximum possible torque and speed in these operations are generally limited by voltage, current ratings, and the neutral point configuration of the motor. To enhance the postfault torque and speed operating region, the torque and speed limits in different postfault operational techniques are determined based on the voltage, current constraints, and neutral point configuration of the SSP-PMSM. In this work, a unified postfault operation is proposed that increases the postfault operational limits by combining MT, ML, and STP operations and modifying the neutral point configuration of the SSP-PMSM. In addition, a technique is also presented that modifies the PWM technique to enable full torque operation below 0.5p.u. speed. The proposed postfault operational technique enables full-speed (1p.u.) operation by operating in STP mode and full torque operation (1p.u.) below 0.5p.u. speed. The postfault operational technique is experimentally validated using a GaN-based 3L-ANPC inverter-driven SSP-PMSM.

Cycle Estimation-Based Deadbeat Interleaving Method for Critical Mode Totem-Pole Rectifiers

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IEEE Transactions on Industrial Electronics
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In totem-pole boost rectifiers, critical mode (CRM) operation is associated with varying switching frequency and duty ratio. This makes it difficult to precisely manage the phase shift between interleaved phases. To address this challenge, we propose a novel interleaving method based on cycle estimation. The switching cycle is estimated by predicting the zero-crossing instants. By analyzing the input current ripple, the relationship among phase shift, duty ratio, and switching cycle can be derived. Therefore, after frequency transition, the phase shift and switching cycle can be updated to provide a precise deadbeat control. Different from conventional methods, the proposed interleaving methods can dynamically modulate the phase shift without the usage of high-speed current sensors. A 1.6 kW, 160--950 kHz GaN-based, two-phase interleaved totem-pole rectifier is designed as the proof of concept. 98.24% peak efficiency and 0.995 power factor are captured. Experimental results effectively validate the interleaving method.

Low Resistivity n-type GaN Ohmic Contacts on GaN Substrates

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In this study, a report is prepared on significantly low specific contact resistivity of alloyed and non-alloyed ohmic contacts fabricated on an as-grown n+-GaN layer and measured with the transfer length method. A low $\rho c = 8 \times 10{-}8\ \Omega\ cm2$ is extracted for the alloyed Ti/Al/Ni/Au, and $\rho c = 4 \times 10{-}7\ \Omega\ cm2$ for the unannealed Ti/Pd/Au. To achieve these, a highly doped n+-GaN layer with $ND = 1.5 \times 1019\ cm{-}3$ is used. The results are derived from a study of three different metal contact stacks, namely Ti/Al/Ni/Au (20 nm/300 nm/20 nm/400 nm), Ti/Pd/Au (2 nm/5 nm/200 nm), and Mo/Au (30 nm/200 nm). The Ti/Al/Ni/Au metal contact is studied in both annealed and non-annealed conditions, whereas for the Ti/Pd/Au and Mo/Au ohmic contacts, a study is conducted without annealing. Their performance and thermal stability are evaluated with a four-probe TLM, with temperatures ranging from 25 to 150 °C. Finally, a theoretical model based on thermionic emission theory is employed to gain a deeper understanding of the physical mechanisms governing the behavior of the ohmic contacts.

A 26-GHz Low Noise Amplifier With 1.6-dB Minimum Noise Figure in 0.15-µm GaN-on-SiC Process

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Microwave and optical technology letters
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A 24.8–29.1-GHz four-stage gallium nitride (GaN) low noise amplifier (LNA) monolithic microwave integrated circuit (MMIC) is presented in this letter which is fabricated in a 0.15-µm GaN-on-SiC process. The proposed GaN LNA utilizes gate/drain bypass networks and source degeneration (SD) to achieve both 0–40-GHz unconditional stability and broadband simultaneous noise and input matching (SNIM). The measured results show a peak gain of 19.9 dB with a 3-dB bandwidth of 4.3 GHz and a low noise figure (NF) of 1.58–2.57 dB. The input and output return losses are better than 11 dB and the output-referred third-order intercept point (OIP3) is greater than 21 dBm. The presented LNA has a core area of 4.2 mm2 and consumes a power dissipation of 150 mW. Compared with other state-of-the-art GaN LNA designs, the proposed LNA exhibits competitive NF and overall performance.

System-Technology Co-Optimization of Multimetal Gated AlGaN/GaN HEMT for Improved RF Linearity

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In this work, a system-technology co-optimization (STCO) of the AlGaN/GaN multimetal gated (MMG) HEMT architecture for third-order transconductance (gm3) engineering and linearity improvement in the presence of fermi-level pinning (FLP) is reported. Through technology computer-aided design (TCAD), compact modeling, load-pull simulations and modulated signal simulations, it is shown that despite incorporating FLP, employing MMG scheme improves device level gm3 -suppression, leading to an improvement in output-referred third-order intercept point per unit dc power (OIP3/PDC) and third order intermodulation distortion (IMD3). Remarkably, OIP3/PDC of 18.9 dB is obtained considering an FLP factor of 0.43, which is a 10.7 dB improvement over the conventional HEMT. MMG HEMT exhibits an output-referred 1-dB compression point (P1-dB) of 3.60 W/mm, compared to 0.60 W/mm for the standard/conventional case. A comparative analysis on output power back-off (OBO) for conventional and MMG HEMT with different FLP factors establishes MMG as a robust architecture to FLP. Simulations involving 5G FR1 signals demonstrate that the adjacent channel power ratio (ACPR) is sustained below –40 dBc up to an output power of 20 dBm. 2.6% lower error vector magnitude (EVM) than baseline case is achieved by MMG HEMT at 5 GHz, under 100 MHz 64-QAM OFDM signals.

High-Yield Enhancement-Mode GaN p-FET With Etching-Target Layer and High-Selectivity Etching Techniques

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This article presents the enhancement-mode (E-mode) GaN p -channel heterojunction field-effect transistors (p -FETs) with p -Al 0.05 Ga 0.95 N etching-target layer (ETL). The optimized high-selectivity etching technique achieves an etch rate of approximately 1 nm/min for p -GaN, while also generating a selectivity ratio of 4:1 between p -GaN and p -Al 0.05 Ga 0.95 N. High-yield E-mode p -FET with ETL has been obtained as the etching process window was expanded to 10 min. The devices achieved the characteristics of a threshold voltage (Vth) of − 1.15 V and a maximum current density (ID,max) of 6.16 mA/mm. Furthermore, the characteristics of multiple devices demonstrate the high consistency and reproducibility of p -FETs' Vth and ION , thus providing significant opportunities for developing complementary circuit integration.

60-dB 70-V/ µ s Three-Stage Op-Amp With Dual Single-Miller Frequency Compensation in GaN-IC Technology

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IEEE Transactions on Circuits and Systems I: Regular Papers
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Modern high-performance electronics is pushing Si technology to its limits. Gallium Nitride (GaN) emerges as a promising alternative due to its superior properties in high-frequency and high-power applications. To fully utilize the fast-switching ability of the GaN technology, monolithic integration is a key. A monolithically integrated GaN power IC (Integrated Circuit) reduces the inductive parasitic enabling a fast

efficient switching operation. However, GaN basic building blocks, particularly operational amplifiers (Op-Amps), face severe challenges due to the limitations of the GaN technology. This paper presents the first three-stage Op-Amp for high-performance feedback circuits realized in the IMEC's 200-V GaN-IC technology on a GaN-on-SOI (Silicon on Insulator) substrate. The design utilizes a cascade of three differential stages resistively loaded to achieve a nearly 60-dB DC gain and 25-MHz gain-bandwidth and implements a novel dual single-Miller frequency compensation technique to provide closed-loop stability. The Op-Amp offers a Slew Rate exceeding 70 V/ μ s with 1% settling time of about 120 ns at room temperature. The correct circuit functionality from − 40 ∘ C to 150 ∘ C was demonstrated through simulations and experimental test.

A Harmonic-Suppressed GaN Power Amplifier Using Artificial Coupled Resonator

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IEEE Transactions on Very Large Scale Integration (VLSI) Systems
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This brief presents an 11.5–17.5-GHz power amplifier (PA) with 32-dBm output power in a 0.25- μ m gallium nitride (GaN) process. Capacitively and inductively coupled resonators are used for impedance matching to achieve a flat in-band power gain and a high out-of-band rejection. Meanwhile, the output matching network provides a second-harmonic suppression to improve the average efficiency within the bandwidth of the PA. The measurements show that the proposed PA exhibits an output power of 31–32.5 dBm and a power gain of more than 10.5 dB from 11.5 to 17.5 GHz. Due to the matching networks providing convenient dc feed and dc block, the chip dimension is only 2.1 × 1.1 mm 2 , corresponding to a power density of 0.77 W/mm 2 . The proposed PA demonstrates a competitive fractional bandwidth and power density in GaN PA monolithic microwave integrated circuits (MMICs).

Monolithic GaN-Based Multiple-Phase Bidirectional Energy Transfer with Seamless Control Applied on High-Voltage and Low-Voltage Batteries

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IEEE Transactions on Circuits and Systems I: Regular Papers
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In this paper, the proposed multi-phase (MP) bidirectional dual Gallium-Nitride (GaN) controlled rectifier (GCR) uses dual GCR with the pre-charge technique to reduce third quadrant operation by minimizing dead time to 0.12ns and 0.13ns, and lowering the negative V DS to − 0.6V and − 0.8V in buck and boost operation, respectively. This work is the first research for monolithic bidirectional energy transfer with a two-switch-only topology. With the help of MP-accelerated current control and the GCR dynamic ramp generator, the voltage variation on the high-voltage (HV) side and low-voltage (LV) side can be reduced to less than 50mV and to 40mV, respectively, during buck and boost operation transitions. Moreover, the recovery time is effectively reduced and current balance between the four phases can be achieved within 7 cycles (= 350ns). The peak efficiency is as high as 95.5% and 94.2% in buck and boost operation, respectively.

Signal-Flow-Based Analysis and Design of Pseudo-Doherty Load-Modulated Balanced Amplifier Toward Unlimited RF Bandwidth

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IEEE Transactions on Microwave Theory and Techniques
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This article reports a first-ever decade-bandwidth pseudo-Doherty load-modulated balanced amplifier (PD-LMBA), designed for emerging 4G/5G communications and multiband operations. By revisiting the load-modulated balanced amplifier (LMBA) theory using an S -matrix-based signal-flow approach, a generalized theory for wideband LMBA operation is developed, taking into account the frequency-dependent nature of all components. In

addition, by analyzing the signal-flow behavior of LMBA, a frequency-agnostic phase-alignment condition is identified as critical for ensuring intrinsic broadband load modulation. This unique design methodology enables, for the first time, the independent optimization of broadband balanced amplifier (BA, as the peaking) and control amplifier (CA, as the carrier), thus fundamentally addressing the longstanding limits imposed on the design of wideband load-modulated power amplifiers (PAs). To prove the proposed concept, an ultrawideband RF-input PD-LMBA is designed and developed using GaN technology covering the frequency range from 0.2 to 2 GHz. Experimental results demonstrate an efficiency of 51% – 72% for peak output power and 44% – 62% for 10 -dB output power back-off (OBO), respectively.

An Efficiency-Enhanced GaN MMIC Nonuniform Distributed Power Amplifier Using a Modified Gate Line Structure

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IEEE Transactions on Microwave Theory and Techniques
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This article introduces a novel four-cell nonuniform distributed power amplifier (NDPA) structure where the amplifier is strategically divided into two main sections with the input power evenly split between them. The input signal of the second section passes through a distributed input matching network (DIMN) instead of the gate line of the first section, as in conventional NDPAs. The lower insertion loss of the DIMN at higher frequencies allows for maintaining the driving voltage of the second section at the same level as the first section. This approach effectively addresses the typical gate line attenuation issue in standard NDPAs that often leads to a decrease in power-added efficiency (PAE) as frequency increases. The proposed structure allows for a distinct tapering method for cell sizing, which can further enhance the NDPA performance. Furthermore, the position of the RF choke has been optimized to mitigate the impact of the output parasitic capacitance from the first cell, thereby enhancing the overall performance of the NDPA at the upper end of the operation band. For verification, a distributed amplifier (DA) was designed and fabricated using a commercial 0.12- μ m gallium nitride (GaN) monolithic microwave integrated circuit (MMIC) process. The amplifier exhibits over 10 dB of small signal gain, 3–4 W of saturated output power, and 28%–45% PAE from 3.5 to 15 GHz. Notably, this amplifier demonstrates a relatively consistent PAE in the upper band of its frequency range.

Compact Reconfigurable Dual-Band MMIC SPDT/SP4T Switches with On-Chip Coupled-Line Structure in GaN-on-SiC HEMT Technology

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This paper presents the design and analysis of dual-band monolithic microwave integrated circuit (MMIC) switches, including a single pole double throw (SPDT) and a single pole four throw (SP4T). With a novel on-chip coupled-line (OCL) topology, the input signal can be switched into low-or high-band paths to create dual-band characteristics. By carefully selecting the electrical lengths of OCLs and device size for corresponding shunt-FETs, the operating frequencies for low-and high-bands can be determined. This brings about improved insertion loss (IL) and isolation (ISO) in a compact structure. With the proposed techniques, two switch prototypes have been designed and fabricated in a 0.25- μ m GaN-on-SiC process for high-power capability. The SPDT consists of a low-band path and a high-band path. It achieves an average IL/ISO of 1.0/32 dB with the best input 1-dB compression points (IP 1dB) of 37.2 dBm at a low-band of DC-15 GHz; and an average IL/ISO of 2.0/28.5 dB with the best IP 1dB of 32.8 dBm at a high-band of 20-40 GHz, respectively. The return loss is better than 11 dB for each port. The SP4T achieves a fully integrated dual-band transmit/receive (T/R) switch with doubled low-/high-band paths. It shows an average IL/ISO of 2.26/27.5 dB

with the best IP 1dB of 31.2 dBm at a low-band of 5-15 GHz; and an average IL/ISO of 2.7/26.5 dB with the best IP 1dB of 30 dBm at a high-band of 20-30 GHz have been achieved, respectively. Better than 11.3 dB return loss is obtained for each port. The chip sizes are 1.8×0.9 mm 2 for the SPDT and 2.2×1.7 mm 2 for the SP4T.

Highly Robust p-GaN Gate HEMT with Surge-Energy Ruggedness under Unclamped Inductive Switching and UV Pulse Laser Irradiation

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IEEE Electron Device Letters
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The robustness of non-avalanche p-GaN gate HEMTs against dynamic overvoltage (V over .) and transient surge-energy (E sur .) shocks is critical for device applications, especially for high-power switching applications. In this work, by carefully constructing an energy dissipating passage from the drain to the source, the proposed device successfully possesses the ability to withstand dynamic overvoltage and safely dissipate surge energy, achieving a maximum V over . of 1.85 kV and an Esur of 11.7 J/cm 2, setting a performance record for GaN-based devices. Furthermore, the device sustains over 1-million times repeated UIS energy shocks, revealing strong robustness. In particular, under extreme conditions of UV pulse laser irradiation and inductive transient, the device still exhibits notable survivability. These results reveal the great potential of non-avalanche p-GaN HEMTs with surge energy dissipating and overvoltage sustaining capabilities for high-power switching applications.

Research on an Inference Algorithm for a Series of Three-Port Converter Topologies

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With the development of sustainable energy industry, aerospace, power electronics technology, and electric vehicles, the demand for energy has become more urgent for humanity. A three port converter (TPC) that can combine photovoltaic cells with batteries has become a better solution at present. However, it is difficult to obtain an ideal TPC. Current TPCs typically have large weight, low efficiency and their topology has a lot of optimization space. This article proposes a topologies inference algorithm for TPC which describes the implementation process of various methods in detail. Different TPC topologies are obtained and experimentally verified. By comparing the different deduction methods proposed, a prototype was developed through branch combination multiplexing. The TPC uses gallium nitride (GaN) high electron mobility transistors (HEMTs) to operate at a frequency of 200 kHz. The power density of it reaches 5.291 W/cm 3 and achieving a 92.8% efficiency with semi-regulated bus architecture.

253 GHz fT Graded-Channel AlGaN/GaN High-Electron-Mobility Transistors with New Cliff Barrier for Millimeter Wave High-Frequency Applications

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In this research work, a graded-channel AlGaN/GaN high-electron-mobility transistor (HEMT) featuring a cliff AlGaN barrier with a gate length of 60 nm is investigated. The inclusion of a foot cliff barrier layer confines the 3DEG distribution, thereby reducing electron scattering and potentially improving carrier mobility. The cliff-graded-channel device shows a peak cutoff frequency fT of 253 GHz and power-added efficiency of 68% at 30 GHz, which represents a significant 60% improvement in comparison with conventional graded-channel devices. These results clearly indicate that the graded-channel AlGaN/GaN HEMT with a new cliff barrier design has great potential for mmW applications.

Design and Verification of a GaN-Based, Single Stage, Grid-Connected Three-Phase PV Inverter

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This research presents the development of a three-phase GaN-based photovoltaic (PV) inverter, focusing on the feasibility, reliability, and efficiency of Gallium Nitride (GaN) technology in solar applications. The study systematically explores the use of GaN Field-Effect Transistors (FETs), particularly in enhancing the efficiency and power density of PV systems. A promising inverter topology was identified and extensively analyzed through comprehensive experiments and design optimisations, resulting in a prototype that achieved a remarkable peak efficiency of 96%. Key aspects of the research included performance benchmarking of GaN FETs, design and testing of LCL filters for grid connection, PCB design considerations for 3-phase inverters, and thorough evaluation of the inverter's performance in terms of power losses, efficiency, and thermal capability. The successful construction and testing of the inverter prototype, despite laboratory constraints, not only demonstrates the viability of GaN over traditional silicon-based inverters but also significantly contributes to advancing renewable energy technologies, paving the way for more efficient and sustainable power systems.

Stability Improvement of GaN Power HEMT by a Multi-Functional Monolithic Protection Circuit

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This work presents a gate electrostatic discharge (ESD) protection circuit monolithically integrated with the GaN power high-electron-mobility-transistor (HEMT). In addition to enhancing the gate robustness against the ESD event, this multi-functional circuit also improves the stability of on-resistance (RON) and threshold voltage (VTH) when power HEMT is under normal switching operations. Such improvement is enabled by clamping the HEMT's negative gate bias (VG) at the OFF state, which is a critical cause of the RON and VTH instabilities in power p-gate GaN HEMTs. A circuit setup is deployed for the in-situ monitoring of the dynamic RON and its evolution from the first switching cycle to the steady state. Under the OFF-state stress with negative VG and high drain bias (VD), the GaN HEMT without ESD circuit shows a drastic dynamic RON increase in the first tens of switching cycles. Such a phenomenon is fully suppressed by the ESD protection circuit. In addition, the longer-term stability of RON and VTH is tested under the prolonged stresses of VG and VD, in which the device with an ESD circuit shows superior stability. Physics-based TCAD simulation unveils the critical physics accounting for such stability improvement. These results reveal a new pathway to address the p-gate GaN HEMTs' inherent instability while simultaneously boosting their gate robustness.

A 15.4-ppm/°C GaN-Based Voltage Reference with Process-Variation-Immunity and High PSR for Electric Vehicle Power Systems

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IEEE Solid-State Circuits Letters
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The proposed gallium nitride (GaN)-based voltage reference (VREF) generator has a low temperature coefficient (TC) of 15.4 ppm/°C, small VREF deviation at different process corners (standard deviation of 0.22%), line sensitivity as low as 0.0023%/V, and high power supply rejection (PSR) of −187 and −114 dB at 100 Hz and 50 MHz, respectively. The proportional-to-absolute-temperature (PTAT) gate current for enhancement-mode GaN (eGaN) optimizes TC. Eliminating depletion-mode GaN (dGaN) gate leakage and using multiple stacked composite dGaNs can improve line regulation and PSR. All performance is achieved with a low power consumption of 10.9 µ W.

Exploring Switching Behavior of Dual-Gate RF GaN HEMTs: Characterization and Modeling

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IEEE Microwave and Wireless Technology Letters
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This letter presents a comprehensive performance analysis and both linear and nonlinear modeling of dual-gate gallium nitride (GaN)-on-silicon (Si) depletion mode high electron mobility transistor (HEMT) devices across various switch topologies. We evaluate large-signal behavior to assess power handling capabilities in three configurations: series, shunt, and single-pole single-throw (SPST) at 6.5 GHz. For the SPST switch at 500 MHz, measurements reveal an on-resistance (Ron) of 2.7 Ω·mm , off-capacitance (Coff) of 53.3 fF, peak insertion loss (IL) of 0.6 dB, and isolation (ISO) of 53.3 dB. These metrics are also evaluated across six different peripheries, ranging from NF · W = 400 to 6400 μ m. In addition, we introduce and validate a surface potential-based modeling framework for dual-gate RF GaN HEMTs using on-wafer dc measurements, common-gate S-parameters, and large-signal measurements. Furthermore, we explore the potential single-pole–double-throw (SPDT) design by utilizing SPST switch S2P files in conjunction with model results.

Compact GaN HEMT Power Amplifier MMIC Delivering Over 40 W for Ku-Band Applications

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IEEE Access
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This paper presents the design and implementation of a high-power amplifier (HPA) using a 250-nm gallium nitride (GaN) high electron mobility transistor (HEMT) process on a silicon carbide substrate. The HPA is engineered to optimize both output power and power density relative to chip size. The 1st and 2nd drive stages utilize individual source via transistors (ISV TRs) for high gain and efficiency, while the output stage employs outside source via transistors (OSV TRs) to achieve high power density. The output matching network is initially designed for a unit TR with a high impedance transformation ratio of 114 and then expanded to a 16-way binary power combining circuit. RC stabilizers with shunt inductors are tailored in the input and interstage matching networks to address the very low input impedance of the drive stage TRs. These stabilizers effectively increase the input impedance of the TRs. The bias circuit is designed with a DC bus-bar structure, enhancing flexibility for large-scale power combining. The fabricated HPA demonstrated a maximum small-signal gain of 26.3 dB at 16.2 GHz and a 3-dB bandwidth ranging from 15.1 to 17.7 GHz. It also achieved an output power of 46.1 dBm (40.7 W) under pulsed operation from 16.0 to 16.75 GHz with a drain voltage of 28 V. When the drain voltage was increased to 32 V, it reached a maximum output power of 63 W at 16.5 GHz, demonstrating an excellent power density of 2.03 W/mm2 per chip area.

Decoupled Double-Channel p-GaN Gate AlGaN/GaN HEMT Featuring Low Reverse Conduction Loss and High Forward Threshold Voltage

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IEEE Electron Device Letters
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A Hybrid-Source p- GaN gate Normally-OFF AlGaN/GaN HEMT is proposed and successfully fabricated, based on a decoupled double-channel structure. It mitigates the compatibility issue between the p- GaN gate and double-channel structures by decoupling the upper and lower channels through a Hybrid-Source structure. Thanks to the source-side Schottky connection to the lower channel, an extremely low reverse turn-ON voltage (-0.5 V) and a large forward threshold voltage (+3.2 V) are simultaneously achieved.

A Transistor-Based Dual-Band Rectifier with Harmonic-Controlled Dual Transmission Line

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IEEE Microwave and Wireless Technology Letters
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This letter proposes a high-efficiency dual-band rectifier based on transistors, introducing a novel output-matching network that integrates harmonic control into the dual-band fundamental impedance-matching design. This approach ensures that the input impedance aligns with the dual-band fundamentals while also effectively expanding the bandwidth of the dual-band rectifier. Additionally, the dual transmission lines modulate the harmonic components of both frequencies into a purely reactive impedance, while the T-section optimizes the imaginary part of the harmonic input impedance for both frequencies. To validate the effectiveness of this method, a high-efficiency dual-band rectifier operating at 0.9 and 2.45 GHz is designed and fabricated using CGH40010F GaN HEMT. Measurement results show that at an input power of 40 dBm and a dc load of 60 Ω , the rectifier achieves efficiencies of 82% at 0.9 GHz and 78% at 2.45 GHz, which maintains a bandwidth of 100 MHz. The circuit size is 6.6 × 4.6 cm.

A Comparative Analysis of Electrical and Optical Thermometry Techniques for AlGaN/GaN HEMTs

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IEEE Transactions on Electron Devices
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Gallium nitride (GaN)-based radio frequency (RF) power amplifiers are spearheading the deployment of next-generation wireless systems owing to the large power handling capability at high frequencies and high-power-added efficiency. Unfortunately, this high power density operation leads to severe overheating, which reduces its lifetime and efficiency. Thus, correctly characterizing the temperature rise is of crucial importance to properly design GaN devices and cooling solutions. Optical-based thermometry techniques such as Raman thermometry and infrared (IR) thermography are commonly used to estimate the peak temperature rise, but they are limited by optical access, topside metallization, and depth averaging. Gate resistance thermometry (GRT) offers an alternative method to measure the temperature without needing optical access to the channel. Therefore, in this work, Raman thermometry is used in conjunction with GRT and electrothermal modeling to determine the accuracy of each method for a field-plated GaN high electron mobility transistor (HEMT) under various bias conditions. While both Raman thermometry and GRT measured a similar temperature rise under fully open (FO) channel conditions, it was found that GRT was better at estimating the peak temperature under a partially pinched-off (PPO) bias condition due to the source-connected field plate (SCFP) restricting optical access to the drain side of the gate edge.

Schottky-MIS Cascode Drain Reverse-Blocking p-GaN Gate Transistor with Significantly Reduced Forward Drop and Ultralow Leakage Current

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IEEE Electron Device Letters
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In this article, we experimentally propose a reverse-blocking (RB) p-GaN gate transistor with the Schottky-MIS cascode drain (CDT) for the significantly reduced forward voltage drop (V F) and ultralow reverse leakage current (I LEAK). At forward bias, electron concentration at the Schottky-MIS cascode drain is higher than that at conventional p-GaN/Ohmic drain, leading to a much lower V F of the Schottky-MIS CDT. When experiencing reverse bias, the Schottky-MIS cascode drain effectively protects the Schottky contact from the high reverse potential compared to Schottky drain, which is beneficial to maintain an ultralow I LEAK in the Schottky-MIS CDT with a p-GaN gate structure. The fabricated Schottky-MIS CDT presents a superior V

F - I LEAK relationship including a greatly reduced V F of 3.1V as well as an ultralow I LEAK of 1×10 -8 A/mm, together with a competitive reverse power figures-of-merits (FOMs) of 120MW/cm 2 . These performances suggest that the proposed Schottky-MIS CDT can be a promising candidate for low-loss RB GaN power transistors and applications requiring a better V F - I LEAK trade-off.

On the Experimental Verification of Electrothermal Modeling of GaN-HEMT-based DC-DC Converters

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IEEE Transactions on Power Electronics
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The reliability of power converters is intricately tied to the variations in the junction temperature of semiconductor devices. Therefore, possessing accurate models of these components is of paramount importance. This research introduces an electrothermal model focusing on Gallium Nitride (GaN) based DC-DC converters. The experimental evaluation leverages a GaN-based Two-Level Buck Converter (TLBC), where current control is achieved via pulse width modulation (PWM), while a comprehensive thermal model is developed in the range of 10 to 500 kHz at fixed switching frequencies. The test-bed involves direct temperature measurement utilizing infrared thermal sensors. The proposed model undergoes validation through comparison with experimental data in steady-state and dynamic conditions. Finally, the contribution of this work is to generate an accurate electrothermal model of a Two-level Buck Converter based on GaN-HEMT technology transistors to enable active thermal control (ATC) implementation in steady-state and dynamic mode. The aim of the study is to address the management of component temperature rise given the need for full integration requirements as a major challenge in new-generation of DC-DC power converters

Deep level transient spectroscopy: Tracing interface and bulk trap-induced degradation in AlGaN/GaN-heterostructure based devices

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Information & Functional Materials
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The exceptional physical properties of gallium nitride (GaN) position GaN-based power devices as leading candidates for next-generation high-efficiency smart power conversion systems. However, GaN's multi-component nature results in a high density of epitaxial defects, whereas the introduction of dielectric layers further contributes to severe interface states and dielectric traps. These factors collectively impair reliability, manifesting as threshold voltage instability and current collapse, which pose significant barriers to the advancement of GaN-based electronics. Establishing the intrinsic relationship between device reliability and defects is crucial for understanding and addressing reliability degradation issue. Deep level transient spectroscopy (DLTS) offers valuable insights by revealing defect-induced changes in electrical parameters during the capture and emission processes under varying biases, thereby elucidating the influence of defects from GaN buffer layers, AlGaN barriers, dielectric layer, and even at dielectric/(Al)GaN interfaces. This research aims to provide a foundational understanding of reliability degradation whereas further enabling enhancements in device performance from the perspectives of epitaxial growth and process preparation, ultimately striving to improve the reliability of GaN-based devices and unlock their full potential for practical applications.

Analysis of trapping effects on DC and RF performance in double Π-gate Al0.3Ga0.7N/GaN MOSHEMTs

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This study investigates trap analysis of the DC and RF performance of Al0.3Ga0.7N/GaN Metal-Oxide-Semiconductor high electron mobility transistor (MOSHEMT) with double π-gate technology. The motivation behind double π-gate technology is to evenly distribute the peak electric field and reduce hot electron generation. This gate design helps to lower hot-electron generation across various operating conditions while maintaining device performance, particularly in the lower millimeter-wave frequency range. High dielectric constant HfO2 is used as gate oxide, which helps to lower the gate leakage current. Near the conduction band (CB), the electron quasi-fermi level of 30 meV is achieved. The practical application of HfO2 in AlGaN/GaN HEMTs is limited by its high oxygen permeability, brittleness, and reactivity with moisture and CO2, which can cause mechanical stress and form hafnium carbonate, adversely affecting device performance. Future designs of the double-π gate structure could enhance electrostatic control, reduce short-channel effects, and improve high-frequency performance by scaling down gate dimensions and using high-k or novel dielectric materials. Additionally, optimization for mm-wave and THz applications would help to maintain electron mobility and minimize parasitic capacitance and resistance.

3D-simulation design of a high current capacity GaN tri-gate power device with integrated parasitic bipolar junction

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Semiconductor Science and Technology
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In this work, a novel high current capability gallium nitride (GaN) tri-gate power device with an integrated parasitic bipolar junction transistor (BJT) is proposed to enhance its static electrical characteristics. The device's electrical characteristics are thoroughly studied and analyzed using 3D technology computer-aided design simulation tools. The two-dimensional electron gas channel is effectively pinched off in the off-state due to the depletion region induced by side-gate metals and parasitic BJT, resulting in a positive threshold voltage (VTH) and enhanced mode (E-mode) operation. The parasitic BJT provides an additional conductive channel in the on-state, significantly improving the output current capability. Compared with the conventional tri-gate (C-Trigate) device, the proposed high current capability GaN trigate (HC-Trigate) device boosts saturation output current by nearly a factor of three under identical conditions, reaching 1,761 mA mm−1. The 3D simulation shows the proposed GaN HC-Trigate power device features a positive VTH of 1.1 V, a low specific on-resistance (Ron,sp) of 0.18 mΩ*cm2 at breakdown voltage of 760 V, and the Baliga's figure of merit of 3.21 GW cm−2. Furthermore, the GaN HC-Trigate power device exhibits superior thermal performance and switching characteristics, indicating its great potential for power electronics applications.

Demonstration and thermal reliability of an e-mode p-type hexagonal boron nitride gate AlGaN/GaN HEMT

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In this letter, we demonstrate an enhancement AlGaN/GaN HEMT with a p-type hexagonal boron nitride (hBN) gate. A major benefit of such structure is that hBN has larger bandgap and critical electric field than GaN, hence the proposed device exhibiting a larger threshold voltage and gate breakdown compared with the conventional p-GaN gate AlGaN/GaN HEMT. In addition, diagrams of p-hBN/AlGaN/GaN heterojunctions can be regulated by a higher Schottky barrier height with a p-hBN gate, leading to a better output performance. Moreover, a better thermal reliability is obtained by the p-hBN gate device with smaller differences of electrical characteristics between room temperature (300 K) and

substrate temperature of 320 K. This can be ascribed to the larger thermal conductivity of hBN, resulting in a much lower temperature in the channel.

Investigation of performance-enhanced GaN-based E-mode p-channel MOSFET with pre-ohmic-annealing treatment

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Pre-ohmic-annealing (POA) treatment of P-GaN/AlN/AlGaN epitaxy under N2 atmosphere was demonstrated to effectively achieve good p-type ohmic contact as well as decreased epitaxy sheet resistance. Ohmic contact resistance (Rc) extracted by transfer length method reduced from 38 to 23 Ω·mm with alleviated contact barrier height from 0.55 to 0.51 eV after POA treatment. X-ray photoelectron spectroscopy and Hall measurement confirmed that POA treatment was able to reduce surface state density and improve the hole concentration of p-GaN. Due to the decreased Rc and improved two-dimensional hole gas (2DHG) density, an outstanding-performance GaN E-mode p-channel MOSFET was successfully realized.

First demonstration of a self-aligned p-channel GaN back gate injection transistor

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In this study, we present the development of self-aligned p-channel GaN back gate injection transistors (SA-BGITs) that exhibit a high ON-state current. This achievement is primarily attributed to the conductivity modulation effect of the 2-D electron gas (2DEG, the back gate) beneath the 2-D hole gas (2DHG) channel. SA-BGITs with a gate length of 1 μm have achieved an impressive peak drain current (ID,MAX) of 9.9 mA/mm. The fabricated SA-BGITs also possess a threshold voltage of 0.15 V, an exceptionally minimal threshold hysteresis of 0.2 V, a high switching ratio of 107, and a reduced ON-resistance (RON) of 548 Ω·mm. Additionally, the SA-BGITs exhibit a steep sub-threshold swing (SS) of 173 mV/dec, further highlighting their suitability for integration into GaN logic circuits.

GaN planar SBD grown and fabricated on SiC substrate with a cutoff frequency of 2.17 THz

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To attain a higher cutoff frequency in GaN planar Schottky Barrier Diodes (SBDs), we investigated the relationship between various structural parameters of the device and its electrical characteristics. Our investigation primarily focused on how the series resistance (Rs) and junction capacitance are affected by the thickness and doping concentration of the N− GaN layer, as well as the anode size, with the goal of improving the diode's operating frequency. The results indicate that by employing an appropriate doping concentration and epitaxial layer thickness, the cutoff frequency of GaN diodes can exceed 2 THz. At last, by increasing the N− GaN doping concentration to 8e17 cm−3 and decreasing the N− GaN layer thickness to 100 nm, the fabricated GaN SBD with a diameter of 1.2 μm and cathode-to-anode distance of 0.8 μm exhibits a series resistance (Rs) of 27.2 Ω and a zero-biased junction capacitance (Cj0) of 2.69 fF, yielding a record cutoff frequency of 2.17 THz. The results suggest that the working frequency of GaN-based multipliers could be further improved for high-power terahertz source applications.

3 kV monolithic bidirectional GaN HEMT on sapphire

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3-kV breakdown voltage was demonstrated in monolithic bidirectional GaN HEMTs having potential applications in 1200V or 1700V-class power converters. The on-resistance of the fabricated transistors was ~20 Ω.mm (~11 mΩ.cm2). The breakdown voltage was optimized with two field plates on either side of the transistor. Shorter first field plate lengths (≤ 2μm) resulted in higher breakdown voltage and the possible reason was discussed. The transistors had a steep subthreshold swing of 92 mV/ dec. The fabricated transistor was benchmarked against the state-of-the-art monolithic bidirectional GaN HEMTs in the performance matrices of breakdown voltage – on resistance, that showed crucial progress.

High performance AlGaN/GaN MISHEMTs using N2O treated TiO2 as the gate dielectric

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In this work, TiO2 thin films deposited by the atomic layer deposition (ALD) method were treated with a special N2O plasma surface treatment and used as the gate dielectric for AlGaN/GaN metal insulator semiconductor high electron mobility transistors (MISHEMTs). The N2O plasma surface treatment effectively reduces defects in the oxide during low-temperature ALD growth. In addition, it allows oxygen atoms to diffuse into the device cap layer to increase the barrier height and thus reduce the gate leakage current. These TiO2 films exhibit a dielectric constant of 54.8 and a two-terminal current of 1.96 × 10−10 A mm−1 in 2 μm distance. When applied as the gate dielectric, the AlGaN/GaN MISHEMT with a 2 μm-gate-length shows a high on/off ratio of 2.59 × 108 and a low subthreshold slope (SS) of 84 mV dec−1 among all GaN MISHEMTs using TiO2 as the gate dielectric. This work provides a feasible way to significantly improve the TiO2 film electrical property for gate dielectrics, and it suggests that the developed TiO2 dielectric is a promising high-κ gate oxide and a potential passivation layer for GaN-based MISHEMTs, which can be further extended to other transistors.

TCAD analysis of gate leakage and threshold drift in GaN devices with dual-gate structure

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Microelectronics Journal
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This article explores the characteristics and performance of a novel high-electron-mobility-transistor (HEMTs) featuring a dual-gate and dual-field plate design. Two-dimensional numerical simulations of the devices were conducted using the semiconductor process simulation software Sentaurus TCAD. The gate reliability issue of p-GaN packaged AlGaN/GaN high electron mobility transistors (HEMTs) was assessed by monitoring the positive gate bias stress time variation from 1μs to 10s. Compared to conventional p-GaN HEMT devices, research simulations show a reduction in gate leakage and an increase in forward gate breakdown voltage from 8.6 V to 11.4 V. Under the parametric conditions described in the text, the reduction in sub-gate resistance results in higher total saturation currents and higher power. This improvement is achieved at the expense of on-resistance and gate capacitance. The simulation results demonstrate that the improvement of the gate by leakage measurement electric field reduces the threshold drift of the device drain bias at 20 V, with the effect of the best forward drift being reduced from 0.2 V to approximately 0.1 V (stress = 10s).

Analysis of On-Resistance in 650-V Enhancement-Mode Active-Passivation p-GaN Gate HEMT

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This work investigates the resistance distribution of the E-mode GaN-on-Si active-passivation (AP) p-GaN gate high-electron-mobility transistor (HEMT) using the transfer length method (TLM). The AP-HEMT has a unique active-passivation layer that is electrically connected to the p-GaN gate and covers most area of the device. The active-passivation layer changes the way the 2DEG is generated in the device, so the constitution of the device RON is expected to differ from the conventional p-GaN gate HEMT (Conv-HEMT). According to our study, the sheet resistance of the 2DEG under the active-passivation layer is lower than that of the access region, leading to the reduced RON in AP-HEMT compared to Conv-HEMT. The temperature dependence of the resistance is also investigated. Additionally, AP-HEMT exhibits an improved reverse conduction performance across the temperature range of 25 °C to 150 °C, due to the reduced gate-to-drain resistance in the device.

2 kV Al0.64Ga0.36N-channel HEMTs with Passivation and Field-Plates

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High voltage (~2 kV) Al0.64Ga0.36N-channel HEMTs were fabricated with on-resistance of ~75 Ω. mm (~21 mΩ. cm2). Two field plates of variable dimensions were utilized to optimize the breakdown voltage. The breakdown voltage reached >3 kV (tool limit) before passivation however it reduced to ~2 kV after Si3N4 surface passivation and field plates deposition. The breakdown voltage and on-resistance demonstrated a strong linear correlation in a scattered plot of ~50 measured transistors. The fabricated transistors were electrically characterized and benchmarked against the state-of-the-art high-voltage (> 1 kV) Al-rich (>40%) AlGaN-channel transistors in breakdown voltage and on-resistance, indicating significant progress.

High-voltage GaN HEMT with self-biased P-GaN VLD layer for improved breakdown voltage and figure of merit

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Microelectronics Journal
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In this article, a novel high-voltage GaN HEMT device with a self-biased multiple stepped P-GaN cap variation lateral doping (VLD) layer is proposed for the first time. The stepped P-GaN VLD layer is self-biased with a voltage of ~5.7 V, preventing depletion of the 2D electron gas in the on-state and maintaining normal current flow. Moreover, it optimizes the surface electric field and increases the breakdown voltage (BV) of the device. Meanwhile, the ohmic contact is formed on the P-GaN layer, hole injection effect occurs in on-state of the device, which suppresses the current collapse effect. The simulation results show that the BV and the specific on-resistance (Ron,sp) of the proposed and conventional devices are 1650 V and 3.1 mΩ cm2, and 650 V and 2.7 mΩ cm2, respectively. The figures of merit (FOM) of the two devices are 0.878 GW/cm2 and 0.156 GW/cm2, which is increased by 462.8 %. The proposed GaN HEMT elevates the BV to over 1200 V-class, along with improved immunity to current collapse.

50nm DrGaN in 3D Monolithic GaN MOSHEMT and Silicon PMOS Process on 300mm GaN-on-Si(111)
Intel Corporation

Power Electronic Devices and Components
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We demonstrate a 50nm DrGaN technology fabricated in a 300mm GaN-on-Silicon process combining E-mode high-k dielectric GaN MOSHEMT with integrated 3D monolithic Si PMOS by layer transfer. The DrGaN consists of a channel-length 50nm GaN MOSHEMT power transistor with figure-of-merit (FOM) of 1.1 (mΩ-nC)-1 and total width of 470.59mm, integrated with a CMOS gate driver comprising a 27.19mm wide 180nm Si PMOS and 49.54mm wide 130nm GaN NMOS. In this work, we employed a gate-last 3D monolithic integration process, where the high temperature activation steps for the Si PMOS transistors are completed before the gate dielectric of the GaN MOSHEMT transistors is deposited.

Enhanced 2DEG confinement in GaN-based HEMTs: Exploring the role of AlGaN back barriers through Schrödinger - Poisson simulations and experimental validation
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Materials Science in Semiconductor Processing
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A systematic investigation, combining simulations and experimental evaluations, for the design of double heterostructures AlxGa1-xN/GaN/AlyGa1-yN and AlN/GaN/AlyGa1-yN high electron mobility transistor (DH-HEMT) structures on a Ga-face GaN (0001) buffer layer on Si (111) substrate, is presented. Self-Consistent Schrödinger-Poisson (SCSP) calculations were implemented for a wide range of composition and thickness values of the AlyGa1-yN back barrier, for the case of an 150 nm GaN channel layer and a top-barrier consisting of either a conventional 30 nm AlGaN (24% AlN) or a 3 nm AlN layer. The SCSP calculations demonstrated the formation of a high energy barrier (2.5–3.0eV) for the transfer of electrons between the channel and the GaN buffer layer/substrate and negligible electron accumulation in the GaN buffer layer, at the bottom AlGaN/GaN interface, when the thickness of the AlGaN back barrier was approximately one-third of the thickness of the GaN channel layer, and the AlN content in the AlGaN alloy of the back barrier was relatively low, not exceeding 10%. The results are explored for the implementation of very thin body AlN/GaN HEMTs on Si (111) by plasma-assisted molecular beam epitaxy. Structures with AlGaN back barriers containing 8% and 30% AlN exhibited similar open channel currents but threshold voltages of −1.2V and −14V, respectively.

Effect of AlN interlayer thickness on thermal conductances of GaN epilayer and GaN/SiC interface in GaN-on-SiC heterostructures
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The temperature rise in GaN-on-SiC based high electron mobility transistors (HEMTs) is firmly dependent on the thermal conductivity (k) of GaN epilayer and the interfacial thermal conductance (G) between GaN and SiC. The AlN buffer is usually utilized during the heteroepitaxial growth of GaN on SiC substrate, while the effects of its thickness on k and G are still not clear. In this study, the GaN/AlN/SiC multilayer structure is prepared by metal–organic chemical vapor deposition, and aiding by time-domain thermoreflectance, we detect how the thickness of AlN interlayer influences k and G. The results reveal

that the AlN interlayer evolves from serrated island shape to smooth planar form with increasing its thickness from 13 to 104 nm, which induces that the tensile stress of the subsequently grown GaN firstly decreases and then increases, giving a minimum value of 339 MPa at 52 nm-thick AlN. Consequently, a maximal k of 150 W m−1 K−1 for the GaN epilayer is achieved. Moreover, the AlN interlayer is beneficial to the enhancement of G due to the improved overlap of phonon density of states, and an increase of G by up to 64 % can be realized via an insertion of 104 nm-thick AlN, which could be the consequence of both atomically smooth interfaces and the improved crystal quality of thicker AlN. The findings clearly manifest the effect of AlN interlayer thickness on the k and G of GaN/AlN/SiC structures, which provides guidelines for preparation of multilayer structures helping to minimize the thermal resistance of HEMTs.

The annealing treatment of interface states in planar and recessed-anode AlGaN/GaN Schottky barrier diodes

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The recessed-anode AlGaN/GaN Schottky barrier diodes (SBDs) were fabricated by self-aligned process, and the effect of annealing of planar and recessed-anode AlGaN/GaN SBDs were investigated. The interface states of AlGaN/GaN SBD were treated by post anode annealing (PAA), which may be attributed to the reduction of metal-induced gap states (MIGS) at Schottky interface. The interface state density (NSS) of planar and recessed-anode AlGaN/GaN SBDs are suppressed by PAA processes to 1.6 × 1013 eV−1cm−2 and 3.9 × 1014 eV−1cm−2, respectively. It is found that after annealing of AlGaN/GaN SBDs, the SBDs stability is enhanced, the leakage current is reduced, the ideal factor is optimized, and the ON-resistance is reduced. The PAA process can effectively improve the performance of AlGaN/GaN SBDs, which is a key technology to optimize GaN SBDs.

Enhancing power density in D-mode GaN HEMT direct-current triboelectric nanogenerators through ICP-etched surface engineering

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In the evolving landscape of energy harvesting, the refinement of friction properties in metal-semiconductor direct current triboelectric nanogenerators (MSDC TENGs) has garnered significant attention. While prior research predominantly concentrated on achieving superior performance in MSDC TENGs through material manipulation, structural adjustments, and friction mode optimization, there has been a noticeable dearth of investigations into surface engineering or modification of semiconductor materials. In this paper, the surface patterning of depletion mode GaN-based high electron mobility transistor (D-GaN HEMT) as friction materials is done by inductively coupled plasma etching method, involving both mechanism analysis and experimental exploration. Through modulation of etching depth and pattern density, a systematically arranged diamond pattern is created on the surface, augmenting surface roughness and charge density. Consequently, the surface-patterned D-GaN HEMT TENG achieves a maximum short-circuit current of 60 μA and a peak power density of 4.05 W/m², which is about 2.8 times greater than the pristine D-GaN HEMT TENG. Furthermore, the power supply capabilities of the surface-patterned D-GaN HEMT TENG are scrutinized, revealing its proficiency in capacitive charging and discharging. The successful activation of a deep ultraviolet LED underscores its potential applications in ultraviolet disinfection. This

research holds substantial significance in optimizing the power generation efficiency and performance of MSDC TENGs employing D-GaN HEMT.

Impact of PECVD deposition on dielectric charge and passivation for n-GaN/SiOx interfaces

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Controlling properties of GaN/dielectric interfaces is crucial for determining the characteristics of MOS-HEMT devices and their stability. Interface properties are largely affected by the techniques and specific conditions of dielectric deposition. In this work, a Taguchi design of experiment was applied to study the effect of plasma parameters during deposition of SiOx by PECVD for passivation of n-GaN. SiOx/GaN MIS capacitors were fabricated and characterized by capacitance measurement at a high probing frequency of 1 MHz. The interface states density, hysteresis and flatband voltage were analyzed and modeled in relation with the flow of SiH4, plasma power, chamber pressure and temperature. Excellent fits could be obtained on a single model including linear terms for all studied parameters and quadratic terms for the flow of SiH4 and temperature. We show that it is possible to obtain some control of the flatband voltage while maintaining a good interface quality. Positive flatband voltages are potentially of interest to enable normally-off operation for MOS-HEMTs and this could be obtained mainly by using a high SiH4/N2O ratio. To the contrary, negative flatband voltage values often ensure the most stable operation of MOS-HEMTs and this was achieved with a low SiH4/N2O and high plasma power. MIS capacitors with near-zero flatband voltage were also obtained with low SiH4/N2O ratio and low plasma power. Hysteresis and interface states density in relation with deposition plasma conditions are also analyzed in order to offer the best trade-offs depending on the end applications of MOS-GaN devices. By demonstrating the great impact of plasma conditions during dielectric deposition on electronic properties of MIS devices, we show that the process of gate insulation can be optimized to simultaneously control the density of defects and fixed charge at the interface.

Ultrafast carrier dynamics in InGaN quantum well channel based HEMT structure

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Ultrafast pump probe measurements on InGaN quantum well (QW) channel based high electron mobility transistor (HEMT) structure enable a direct measurement of the transit/capture time of electrons from GaN buffer layer to InGaN channel layer. Carrier capture time of 75 ± 10 fs is measured and the same is found to be independent of excitation wavelength. However, the capture process is delayed by 160 ± 5 fs when carriers are excited in GaN buffer layer. This happens due to the inclusion of transit time of carriers in GaN layer. It is confirmed by varying the wavelength of excitation where a delay in carrier transit is seen at longer wavelength. It is also seen that the strength of a feature associated with the carriers excited in GaN layer and captured by InGaN QW channel layer mimics the absorption spectrum of GaN, which also confirms that the delay in capture process is caused by the carriers excited in GaN layer. It is found that the capture process can be delayed even up to 240 ± 5 fs when the pump wavelength is kept at 390 nm. It is explained by considering the absorption in a deeper part of GaN layer and via the shallow defect states. Further, it is found that the localization of carriers in InGaN QW channel layer occurs at the time scales of 85 ± 10 fs. The transit/capture/localization time parameters reported in this work provide a crucial set

of information, which is essential for modulating the carrier dynamics in InGaN/GaN based HEMTs and other high speed optoelectronic devices.

Unveiling the abnormal response behavior of AlGaN-based high electron mobility transistors (HEMTs) under ultraviolet light illumination

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This study examines the dual functionality of AlGaN/GaN HEMTs as both power transistors and UV photodetectors, motivated by manipulating the bias dependent photoresponse and to perform both functions using AlGaN/GaN HEMT configuration seamlessly. The fabricated HEMTs achieve good electrical performance, with a maximum drain current IDS of 547 mA/mm and an ON-to-OFF current ratio (ION/IOFF) of 1.2×10^7, with a threshold voltage of −3.9 V. The device demonstrated a peak responsivity of 758.4 A/W at 360 nm with an optical gain of 2617 under forward bias. When biased between −4.6 V < VGS < Vth and VDS = +3 V, UV illumination significantly increases the 2DEG channel conductivity, resulting in enhanced electron transport and high responsivity. However, as VGS increases, dark current rises, limiting the gain improvement. Additionally, the proposed AlGaN HEMTs showed a UV sensing performance with a linear dynamic range (LDR) of 65.4 dB, indicating potential for UV detection applications. Furthermore, these devices can also operate in reverse conduction (third quadrant), achieving 220.7 A/W when VDS < 0 V and VGS + VSD > Vth. Applying a higher drain-source voltage further boosts responsivity by strengthening the lateral electric field, but only if dark current remains low. Finally, the HEMTs detect optical pulses at 550 Hz with response times of 641 µs and 776 µs (τr/τf). These capabilities allow the device to function as both a power signal driver and an optical detector without structural modifications, making it a versatile option for multifunctional applications.

Fe-doped buffer layer with graded layered AlGaN/GaN HEMT for millimeter-wave radar applications

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The low cost and scalability of silicon substrates have led to increasing attention to AlGaN/GaN high-electron-mobility transistors (HEMTs) on silicon wafer. We developed and simulated the GaN-based HEMT on Si wafer using the Silvaco TCAD software. The performance of rectangular-gate AlGaN/GaN HEMT on Si wafer is examined in detail with respect to the effects of channel length variation, barrier thickness variation, and gate length variation. The performance of this HEMT structure with a gate length of 100 nm and optimized channel layer thickness (CT) of 200 nm has shown a significant IDS of 1.11 A/mm, a substantial Gm of 329.79 mS/mm, an impressive fT of 199.40 GHz, and a notable output current of 1.71 A/mm. When the barrier layer thickness (BT) was varied from 6 to 10 nm while maintaining a 200 nm channel layer thickness, the performance declined at higher barrier thicknesses, yielding an IDS of 0.8 A/mm, a Gm of 206 mS/mm, an fT of 193.2 GHz, and an output current of 1.26 A/mm. Finally, this HEMT structure demonstrated superior performance with a gate length (LG) of 40 nm, exhibiting a drain current of 1.92 A/mm, a transconductance (Gm) of 465.49 mS/mm, and a cut-off frequency (fT) of 465 GHz, and output current (ID) of 2.11 A/mm. The optimized device structure's high-

power performance without compromising RF performance, they are suitable for millimeter-wave radar applications.

The Influence of AlGaN Spacer Thickness on the Electrical Properties of InAlN/AlGaN/AlN/GaN Heterostructure

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InAlN is particularly suitable for applications in high-power electronic devices because it has a higher polarization than traditional barrier layer materials and can achieve no lattice constant mismatch between GaN and InAlN. However, the InAlN epitaxial layer alloy disorder is difficult to improve, which will seriously affect the mobility of two-dimensional electron gas (2DEG) formed by InAlN/GaN heterostructures. In this paper, two groups of GaN-based heterostructures have been fabricated to study the influence of InAlN thickness and AlGaN thickness on the In0.17Al0.83N/Al0.23Ga0.77N/AlN/GaN heterostructure electrical properties. A wide range of 2DEG sheet density from 1.12 × 1013 to 1.92 × 1013 cm−2 was achieved while the mobility varied from 1064 to 1945 cm2/V s. Both the 2DEG mobility and the surface flatness improved a lot with the increase of the Al0.23Ga0.77N thickness. The heterostructure with 16 nm InAlN shows a higher electron mobility and 2DEG sheet density compared with that with 8 nm InAlN. In addition, there exists a proper thickness of AlGaN spacer to strike a balance between the 2DEG mobility and sheet density to achieve the lowest sheet resistance. The proper thickness is around 2–4 nm which will keep the sheet resistance in a low level.

High current density heterojunction bipolar transistors with 3D-GaN/2D-WSe2 as emitter junctions

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Materials Horizons
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With the continuous advancement of electronic technology, there is an increasing demand for high-speed, high-frequency, and high-power devices. Due to the inherently small thickness and absence of dangling bonds of two-dimensional (2D) materials, heterojunction bipolar transistors (HBTs) based on 2D layered materials (2DLMs) have attracted significant attention. However, the low current density and limited structural design flexibility of 2DLM-based HBT devices currently hinder their applications. In this work, we present a novel vertical GaN/WSe2/MoS2 HBT with three-dimensional (3D)-GaN/2D-WSe2 as the emitter junction. Harnessing the high carrier concentration and wide bandgap of 3D-GaN, an HBT with a current density of about 260 A cm−2 is obtained. In addition, by selecting an adequate position for the collector electrode, we achieve efficient carrier collection through a collector junction smaller than the emitter junction area, obtaining a common–base current gain of 0.996 and a remarkable common–emitter current gain of 12.4.

Normally-Off Trench-Gated AlGaN/GaN Current Aperture Vertical Electron Transistor with Double Superjunction

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Technologies
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This study proposes an AlGaN/GaN current aperture vertical electron transistor (CAVET) featuring a double superjunction (SJ) to enhance breakdown voltage (BV) and investigates its electrical characteristics via technology computer-aided design (TCAD) Silvaco Atlas simulation. An additional p-pillar was formed beneath the gate current blocking layer to create a

lateral depletion region that provided a high off-state breakdown voltage. To address the tradeoff between the drain current and off-state breakdown voltage, the key design parameters were carefully optimized. The proposed device exhibited a higher off-state breakdown voltage (2933 V) than the device with a single SJ (2786 V), although the specific on-resistance of the proposed method (1.29 mΩ·cm−2) was slightly higher than that of the single SJ device (1.17 mΩ·cm−2). In addition, the reverse transfer capacitance was improved by 15.6% in the proposed device.

Enhancing Resistive Switching in AlN-Based Memristors Through Oxidative Al2O3 Layer Formation: A Study on Preparation Techniques and Performance Impact

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Aluminum nitride (AlN) with a wide band gap (approximately 6.2 eV) has attractive characteristics, including high thermal conductivity, a high dielectric constant, and good insulating properties, which are suitable for the field of resistive random access memory. AlN thin films were deposited on ITO substrate using the radio-frequency magnetron sputtering technique. Al's and Au's top electrodes were deposited on AlN thin films to make a Au/Al/AlN/ITO sandwich structure memristor. The effects of the Al2O3 film on the on/off window and voltage characteristics of the device were investigated. The deposition time and nitrogen content in the sputtering atmosphere were changed to adjust the thickness and composition of AlN films, respectively. The possible mechanism of resistive switching was examined via analyses of the electrical resistive switching characteristics, forming voltage, and switching ratio.

The Trapping Mechanism at the AlGaN/GaN Interface and the Turn-On Characteristics of the p-GaN Direct-Coupled FET Logic Inverters

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Nanomaterials
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The trapping mechanism at the AlGaN/GaN interface in the p-GaN high electron mobility transistors (HEMTs) and its impact on the turn-on characteristics of direct-coupled FET logic (DCFL) inverters were investigated across various supply voltages (VDD) and test frequencies (fm). The frequency-conductance method identified two trap states at the AlGaN/GaN interface (trap activation energy Ec-ET ranges from 0.345 eV to 0.363 eV and 0.438 eV to 0.47 eV). As VDD increased from 1.5 V to 5 V, the interface traps captured more electrons, increasing the channel resistance (Rchannel) and drift-region resistance (Rdrift) of the p-GaN HEMTs and raising the low-level voltage (VOL) from 0.56 V to 1.01 V. At fm = 1 kHz, sufficient trapping and de-trapping led to a delay of 220 µs and a VOL instability of 320 mV. Additionally, as fm increased from 1 kHz to 200 kHz, a positive shift in the threshold voltage of p-GaN HEMTs occurred due to the dominance of trapping. This shift caused VOL to rise from 1.02 V to 1.40 V and extended the fall time (tfall) from 153 ns to 1 µs. This investigation enhances the understanding of DCFL GaN inverters' behaviors from the perspective of device physics on power switching applications.

Emerging Technologies for Advanced Power Electronics and Machine Design in Electric Drives

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Appl. Sci.
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The paper presents a comprehensive overview of recent advancements in power electronics and electric machine design, focusing on novel topologies, semiconductor technologies, and integrated design techniques for electric drives. New drive topologies are gradually moving from the research phase to practical application, aiming to increase the rated power, efficiency, and reliability of electric drives. Specifically, these topologies can be categorized into series, which focus on increasing the operating voltage; parallel, which aim at enhancing the operating current and adding redundancy; and multiphase, known for offering significant benefits such as improved fault tolerance, higher torque generation, the possibility of synthetic loading, and diverse winding layout options. Emerging wide bandgap semiconductors, such as silicon carbide and gallium nitride, allow for operation at higher frequencies and lower power losses, enabling further drive integration. In terms of design practices, higher computational power, supported by advanced software, enables simulation and analysis in multiple domains (thermal, mechanical, electromagnetic) using multiphysics co-simulation, as well as multi-objective optimization concepts to achieve rapid prototyping of optimized drive systems. All the approaches described are important steps towards further improving electric drives for numerous applications in industry, consumer electronics, and transportation.

Damping of Flying Capacitor Dynamics in Multi-Level Boost DC-DC Converters

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Electronics
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This paper presents a novel modeling approach for flying capacitor dynamics in boost-type multi-level converters (FCML-boosts) controlled by Phase Shift Pulse Width Modulation (PSPWM). By explicitly taking into account the interaction between the inductor current and the flying capacitor voltage, the model is able to reveal an underlying resonance phenomenon and to predict its frequency at each operating point. Based on such a model, whose derivation is explained in detail, both passive and active damping solutions are proposed, designed, and experimentally verified that significantly reduce the undesirable oscillations. The analytical results and the devised control solutions are tested on a 1kW, four-level, boost DC-DC converter prototype employing 200V, 48A rated EPC2034C GaN devices.

Broadband Millimeter-Wave Front-End Module Design Considerations in FD-SOI CMOS vs. GaN HEMTs

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Millimeter-wave (mm-Wave) phased array systems need to meet the transmitter (Tx) equivalent isotropic radiated power (EIRP) requirement, and that depends mainly on the design of two key sub-components: (1) the antenna array and (2) the Tx power amplifier (PA) in the front-end-modules (FEMs). Simulations using an electromagnetic (EM) solver carried out in Cadence AWR with AXIEM suggest that for two uniform square patch antenna arrays at 24 GHz, the 4 element array has ~6 dB lower antenna gain and twice the half power beam width (HPBW) compared to the 16 element array. We also present measurements and post-layout parasitic-extracted (PEX) EM simulation data taken on two broadband mm-Wave PAs designed in our lab that cover the key portions of the fifth-generation (5G) FR2-band (i.e., 24.25–52.6 GHz) that lies between the super-high-frequency (SHF, i.e., 3–30 GHz) band and the extremely-high-frequency (EHF, i.e., 30–300 GHz) band: one designed in a 22 nm fully depleted silicon on insulator (FD-SOI) CMOS process, and the other in an advanced 40 nm Gallium Nitride (GaN) high-electron-mobility transistor (HEMT) process. The FD-SOI PA achieves saturated output power (POUT,SAT) of ~14 dBm and peak power-added efficiency (PAE) of ~20% with ~14 dB of gain and 3 dB bandwidth (BW) from

~19.1 to 46.5 GHz in measurement, while the GaN PA achieves measured POUT,SAT of ~24 dBm and peak PAE of ~20% with ~20 dB gain and 3 dB BW from ~19.9 to 35.2 GHz. The PAs' measured data are in good agreement with the PEX EM simulated data, and 3rd Watt-level GaN PA design data are also presented, but with simulated PEX EM data only. Assuming each antenna element will be driven by one FEM and each phased array targets the same 65 dBm EIRP, millimeter wave (mm-Wave) antenna arrays using the Watt-level GaN PAs and FEMs are expected to achieve roughly 2× wider HPBW with 4× reduction in the array size compared with the arrays using Si FEMs, which shall alleviate the thorny mm-Wave line-of-sight (LOS)-blocking problems significantly.

Electro-Thermal Co-Optimization Design of GaN MMIC PA

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Electronics
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A method of electro-thermal co-optimization design for the Gallium nitride (GaN) monolithic microwave integrated circuit (MMIC) power amplifier (PA) is introduced in this paper. Due to the self-heating effect of the GaN high electron mobility transistor (HEMT), it is necessary to pay attention to the influence of thermal resistance change on circuit performance when designing a high-power RF PA. For this purpose, a three-dimensional finite element analysis model of GaN multi-gate HEMT is developed. The thermal resistance and junction temperature of the device under a RF dynamic current are extracted by heat transfer simulation and can be substituted into the temperature node of the transistor model for PA circuit simulation design. To verify the proposed method, a Class AB MMIC PA was designed and tested using a 0.15-µm GaN-on-SiC process. Through the application of the above methods, the designed PA performance is optimized and achieves the performance of over 60% power-added efficiency (PAE) and 38 dBm saturation power (Psat) within a compact area of 1.6 mm × 2.2 mm. It is demonstrated that the proposed method can effectively improve the consistency of simulation results and measurement results, which can be a valuable reference for high-power MMIC PA design.

Development of GaN-Based, 6.6 kW, 450 V, Bi-Directional On-Board Charger with Integrated 1 kW, 12 V Auxiliary DC-DC Converter with High Power Density

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Micromachines
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Automotive-grade GaN power switches have recently been made available in the market from a growing number of semiconductor suppliers. The exploitation of this technology enables the development of very efficient power converters operating at much higher switching frequencies with respect to components implemented with silicon power devices. Thus, a new generation of automotive power components with an increased power density is expected to replace silicon-based products in the development of higher-performance electric and hybrid vehicles. 650 V GaN-on-silicon power switches are particularly suitable for the development of 3–7 kW on-board battery chargers (OBCs) for electric cars and motorcycles with a 400 V nominal voltage battery pack. This paper describes the design and implementation of a 6.6 kW OBC for electric vehicles using automotive-grade, 650 V, 25 mΩ, discrete GaN switches. The OBC allows bi-directional power flow, since it is composed of a bridgeless, interleaved, totem-pole PFC AC/DC active front end, followed by a dual active bridge (DAB) DC-DC converter. The OBC can operate from a single-phase 90–264 Vrms AC grid to a 200–450 V high-voltage (HV) battery and also integrates an auxiliary 1 kW DC-DC converter to connect the HV battery to the 12 V battery of the vehicle. The auxiliary DC-DC converter is a center-tapped phase-shifted full-bridge (PSFB) converter with synchronous rectification. At the low-voltage side of the auxiliary converter, 100 V GaN power switches are used. The entire OBC is liquid-cooled. The first prototype of the OBC exhibited a 96% efficiency and 2.2 kW/L power density (including the cooling system) at a 60 °C ambient temperature.

TCAD Simulation of an E-Mode Heterojunction Bipolar p-FET with Imax > 240 mA/mm

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This work demonstrates an enhancement mode heterojunction bipolar p-FET (HEB-PFET) structure with a AlGaN/GaN heterojunction bipolar transistor (HBT) integrated on the drain side. Such device design notably contributes to the ultra-high output current density, which is conventionally limited by the low hole mobility and concentration in the p-FETs. The HEB-PFET exhibits an output current density of 241 mA/mm, which is 134 times larger compared to the conventional p-FET (C-PFET) and 2.4 times of the homojunction bipolar p-FET (HOB-PFET). This can be attributed to a better current gain of HBT than homojunction bipolar transistor (BJT). An optimized HEB-PFET of 6 nm p-GaN layer beneath the gate is proposed, where ION/IOFF is >1011, and Vth is −0.44 V. Additionally, thermal stabilities are studied with temperature changes from 300 K to 425 K. Moreover, a semi-empirical compact model is presented to visually explain the working principle of the HEB-PFET.

750 V Breakdown in GaN Buffer on 200 mm SOI Substrates Using Reverse-Stepped Superlattice Layers

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Micromachines
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In this work, we demonstrated the epitaxial growth of a gallium nitride (GaN) buffer structure on 200 mm SOI (silicon-on-insulator) substrates. This epitaxial layer is grown using a reversed stepped superlattice buffer (RSSL), which is composed of two superlattice (SL) layers with different Al component ratios stacked in reverse order. The upper layer, with a higher Al component ratio, introduces tensile stress instead of accumulative compressive stress and reduces the in situ curvature of the wafer, thereby achieving a well-controlled wafer bow ≤ ±50 µm for a 3.3 µm thick buffer. Thanks to the compliant SOI substrate, good crystal quality of the grown GaN layers was obtained, and a breakdown voltage of 750 V for a 3.3 µm thick GaN buffer was achieved. The breakdown field strength of the epitaxial GaN buffer layer on the SOI substrate is estimated to be ~2.27 MV/cm, which is higher than the breakdown field strength of the GaN-on-Si epitaxial buffer layer. This RSSL buffer also demonstrated a low buffer dispersion of less than 10%, which is good enough for the further processing of device and circuit fabrication. A D-mode GaN HEMT was fabricated on this RSSL buffer, which showed a good on/off ratio of ~109 and a breakdown voltage of 450 V.

Accurate Evaluation of Commutations of 650 V GaN Power Switches Assisted by Electromagnetic Simulations in a 7 kW Dual Active Bridge Converter for Automotive Battery Charging Applications

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Electronics
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The exploitation of high-voltage GaN power switches enables the development of power converters with superior characteristics with respect to components developed with heritage silicon-based technologies. One of the key advantages of GaN switches is their very fast commutation capability due to reduced parasitic capacitance and inductance with respect to silicon devices. The capability of an accurate evaluation of the switch commutations in the design phase is of crucial importance to maximize performance and avoid reliability or electromagnetic compatibility issues in the final converter. In this paper, an accurate evaluation of high-voltage GaN HEMT commutations is performed, exploiting detailed non-

linear dynamic models of transistors and electromagnetic simulations of a PCB. A deep insight into the commutation waveforms in the intrinsic device (i.e., conductive drain current and intrinsic node voltages) is proposed to evaluate and explain the mechanisms of almost lossless turn-off and turn-on commutations in a 7 kW DAB converter. The influence on the performance of the PCB parasitics and the driver characteristics are accurately reproduced by simulations, suggesting important guidelines for the optimal design of power converters fully exploiting GaN HEMT's potential. This detailed simulation/analysis approach for transistor commutation is typically adopted in Radio Frequency amplifier design but also becomes very valuable in power converter design when the very fast commutations of a GaN HEMT at a high switching frequency cannot be fully described and taken under control with conventional approaches used in power electronics design. The simulation results are confirmed by experimental data.

A Study of Reverse Characteristics of GaN-on-Si Quasi-Vertical PiN Diode with Beveled Sidewall and Fluorine Plasma Treatment

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Micromachines
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In this work, we show a high-performance GaN-on-Si quasi-vertical PiN diode based on the combination of beveled sidewall and fluorine plasma treatment (BSFP) by an inductively coupled plasma (ICP) system. The leakage current and breakdown voltage of the diode are systematically studied. Due to the beveled sidewall treated by the fluorine plasma, the diodes achieve an excellent breakdown voltage (VBR) of 790 V and a low reverse leakage current. In addition, the GaN-on-Si quasi-vertical PiN diode achieves a low specific on-resistance (Ron,sp) of 0.51 mΩ·cm2 and a high Baliga's figure of merit (BFOM) of 1.22 GW/cm2. The relationship between the total leakage current and the device diameter shows that the sidewall leakage is the main leakage path of the device. Afterwards, the TCAD simulations based on electric field and electric potential reveal that the fluorine plasma treatment is a major factor in suppressing the leakage current and increasing the VBR for a diode with BSFP. This work systematically analyzes the effects of beveled sidewall and fluorine plasma treatment based on the reverse characteristics of the GaN-on-Si quasi-vertical PiN diode and highlights the great potential of the GaN-on-Si PiN diode for various power applications.

A Novel ANN-PSO Method for Optimizing a Small-Signal Equivalent Model of a Dual-Field-Plate GaN HEMT

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Micromachines
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This study introduces a novel method that integrates artificial neural networks (ANNs) with the Particle Swarm Optimization (PSO) algorithm to enhance the efficiency and precision of parameter optimization for the small-signal equivalent model of dual-field-plate GaN HEMT devices. We initially train an ANN model to predict the S-parameters of the device, and subsequently utilize the PSO algorithm for parameter optimization. Comparative analysis with the NSGA2 and DE algorithms, based on convergence speed and accuracy, underscores the superiority of the PSO algorithm. Ultimately, this ANN-PSO approach is employed to automatically optimize the internal parameters of a 4 × 250 µm dual-field-plate GaN HEMT equivalent circuit model within the frequency range of 1–18 GHz. The method's effectiveness under varying bias conditions is validated through comparison with traditional physical formula analysis methods. The results demonstrate that the ANN-PSO method significantly enhances the automation and efficiency of parameter optimization while maintaining model accuracy, providing a reference for the optimization of other device models.

Continuously Beam-Steered Phased Array Antenna Using GaN Varactors for Millimeter-Wave Applications

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A continuously steerable beam patch antenna array employing a classical phase shifter based on GaN HEMTs is presented. Here, the GaN HEMTs are used as varactor diodes to achieve the tunability purpose. By controlling the DC bias of these varactors from −2 V to 2 V, the proposed array antenna can provide continuous beam steering from 0° to +25° in the azimuth plane at 41.20 GHz, while achieving a low side-lobe level and good impedance matching performances. Using GaN HEMTs as varactors to achieve beam steering capability has never been tried before to the best of our knowledge. The measurement results agree well with the simulation results and validate the effectiveness of the proposed beam steering based on GaN technology. This proposed phased array antenna will find numerous applications within future wireless communications systems, especially for millimeter-wave applications.

Band Alignment of AlN/InGaZnO Heterojunction for Thin-Film Transistor Application

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Electronics
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Uncrystallized indium-gallium-zinc-oxide (InGaZnO) thin-film transistors (TFTs) combined with an aluminum nitride (AlN) dielectric have been used to promote performance and steadiness. However, the high deposition temperature of AlN films limits their application in InGaZnO flexible TFTs. In this work, AlN layers were deposited via low-temperature plasma-enhanced atomic layer deposition (PEALD), and InGaZnO films were fabricated via high-power impulse magnetron sputtering (HIPIMS). The band alignment of the AlN/InGaZnO heterojunction was studied using the X-ray photoemission spectrum and ultraviolet visible transmittance spectrum. It was found that the AlN/InGaZnO system exhibited a staggered band alignment with a valence band offset ΔEv of −1.25 ± 0.05 eV and a conduction band offset ΔEc of 4.01 ± 0.05 eV. The results imply that PEALD AlN could be more useful for surface passivation than a gate dielectric to promote InGaZnO device reliability under atmospheric exposure.

Probing electron trapping by current collapse in GaN/AlGaN FETs utilizing quantum transport characteristics

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GaN is expected to be a key material for next-generation electronics due to its interesting properties. However, current collapse poses a challenge to the application of GaN FETs to electronic devices. In this study, we investigate the formation of quantum dots in GaN FETs under current collapse. By comparing the Coulomb diamond between standard measurements and those under current collapse, we find that the gate capacitance is significantly decreased under current collapse. This suggests that the current collapse changes the distribution of trapped electrons at the device surface, as reported in the previous study by operando x-ray spectroscopy. In addition, we show external control of quantum dot

formation, previously challenging in an FET structure, by using current collapse.

Research on RF performance of GaN HEMT with graded Al composition AlGaN back-barrier

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Micro and Nanostructures
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In this paper, we apply AlGaN back-barrier with graded Al composition to effectively improve the RF performance of GaN high electron mobility transistor (HEMT). Simulation results demonstrate that compared with GaN HEMT with fixed Al composition AlGaN back-barrier, graded AlGaN back-barrier HEMT has lower gate capacitance and better two-dimensional electron gas (2DEG) confinement. Its cut-off frequency (ft) and maximum oscillation frequency (fmax) reach 100 GHz and 179.8 GHz, respectively, an increase of 12.1 GHz and 42.9 GHz. Due to the lower power supply, graded AlGaN back-barrier HEMT also significantly improves the power added efficiency (PAE) compared with HEMT without back-barrier, increasing 20 %. Moreover, it is found that graded AlGaN back-barrier HEMT has better large-signal performance than fixed AlGaN back-barrier HEMT for the better electron confinement.

Improvement of recessed MOS gate characteristics in normally-off AlN/GaN MOS-HFETs with N2/NH3 thermal treatment

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This study investigated the metal–oxide–semiconductor gate characteristics of recessed-gate AlN/GaN metal–oxide–semiconductor-heterojunction-field-effect transistor with N2/NH3 thermal treatment. The gate-channel mobility in recessed-gate structures formed by the inductively coupled plasma-reactive ion etching method is degraded due to plasma-induced damage. The application of thermal treatment to etch-damaged GaN surfaces was observed to re-form a clear step-terrace structure, effectively reversing the effects of the etching damage. A corresponding enhancement in peak field-effect mobility was experimentally verified, with an increase from a pretreatment value of 656 to 1042 cm2/V.s after thermal treatment. Concurrently, an improvement of the lower gate-leakage current by 1–2 orders of magnitude was measured. This thermal treatment method can reduce crystal defects at deep levels of 1.8–2.9 eV below Ec on the etched GaN surface. In particular, this N2/NH3 thermal treatment approach could potentially contribute to the reduction of deep levels such as atomic displacement, gallium vacancies, and those complexes generated by inductively coupled plasma-reactive ion etching.

Polarization-induced two-dimensional hole gases in N-polar AlGaN/GaN heterostructures

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We report the observation of two-dimensional hole gases (2DHGs) in N-polar AlGaN/GaN heterostructures grown on single-crystal GaN substrates by plasma-assisted molecular beam epitaxy. A systematic study varying AlGaN barrier thickness is performed. The presence of 2DHGs is confirmed by persistent p-type conductivity and high hole mobility observed in temperature-dependent Hall-effect measurements down to 10 K, and the dependence of 2DHG density on the AlGaN barrier thickness indicates its polarization induced origin. 2DHG with a sheet density of 7.5x10^12 cm−2 shows a relatively high hole mobility of 273 cm2 V−1 s−1 at 10 K. Mobility model fit suggests that acoustic phonon scattering is the dominant scattering mechanism in the sub-room temperature region. This work indicates that the quality of N-polar 2DHGs is comparable to that of state-of-the-art metal-

polar 2DHGs, contributing to a building block for potential high-quality N-polar p-channel devices.

1500 V recessed-free GaN-based HEMTs with ultrathin barrier epitaxial structure

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This Letter demonstrates a 1500-V enhancement-mode (E-mode) GaN-based high electron mobility transistors (HEMTs) based on the recessed-free structure. The E-mode GaN-based HEMTs fabricated based on the ultrathin barrier epitaxial structure have a small gate interface traps density (Dit) of ∼1012 cm−2 eV−1, which can be attributed to the avoidance of AlGaN etching in the gate region. Meanwhile, a small threshold voltage (Vth) hysteresis of 19 mV and a small subthreshold swing of 101 mV/dec are achieved in the fabricated devices with a Vth around 1.91 V. A small Vth shift of 0.05 V was achieved under positive gate voltage stress, indicating that the devices have good Vth stability. Meanwhile, a high yield of more than 90% has been achieved on 6-in. wafer, which provides a good scheme for the commercialization of E-mode HEMTs.

High-performance AlGaN/GaN HEMTs with Hf0.5Zr0.5O2-based ferroelectric gate by pulsed laser deposition

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This Letter demonstrates AlGaN/GaN high-electron-mobility transistors (HEMTs) with Hf0.5Zr0.5O2 (HZO) ferroelectric gate dielectric using pulsed laser deposition (PLD). An ultrathin Al2O3 interlayer grown by atomic layer deposition is used to avoid destroying the AlGaN surface and decreasing the electron density of a two-dimensional electron gas channel before PLD. The high-quality HZO on AlGaN/GaN heterostructure contributes to the good insulating and ferroelectric properties of the HZO film, yielding a superior ON/OFF current ratio of 4 × 1011 and a low sub-threshold slope (SS) of 53.2 mV/dec. Moreover, the electrical characteristics of the device are systematically investigated before and after gate poling. In combination with the analysis of schematic band diagrams, we found that ferroelectric polarization can effectively regulate the capture and release processes of channel electrons by Al2O3/AlGaN interface defects. These results show that HZO-based ferroelectric HEMTs have great potential for high frequency, low power consumption, and multi-functional devices.

Demonstration of Si-doped Al-rich regrown Al(Ga)N films on AlN/sapphire with >10^{15}/cm^3 carrier concentration using CCS-MOCVD reactor

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https://doi.org/10.1063/5.0231960

Thin Si-doped Al-rich (xAl > 0.85) regrown Al(Ga)N layers were deposited on AlN on sapphire template using metal-organic chemical vapor deposition (MOCVD) techniques. The optimization of the deposition conditions, such as temperature (1150 °C), V/III ratio (750), deposition rate (0.7 Å/s), and Si concentration (6 × 1019/cm3), resulted in a high charge carrier concentration (> 1015 cm−3) in the Si-doped Al-rich Al(Ga)N films. A pulsed deposition condition with pulsed triethylgallium and a continuous flow of trimethylaluminum and ammonia was employed to achieve a controllable Al composition xAl > 0.95 and to prevent unintended Ga incorporation in the AlGaN material deposited using the close-coupled showerhead reactor. Also, the effect of unintentional Si incorporation on free charge carrier concentration at the regrowth interface was studied by varying the thickness of the regrown Al(Ga)N layer from 65 to <300 nm. A maximum charge carrier concentration of

4.8 × 1016 and 7.5 × 1015/cm3 was achieved for Al0.97Ga0.03N and AlN films with thickness <300 nm compared to previously reported n-Al(Ga)N films with thickness ≥400 nm deposited using MOCVD technique.

P-type NiOX dielectric-based CMOS inverter logic gate using enhancement-mode GaN nMOS and diamond pMOS transistors

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Appl. Phys. Lett.
https://doi.org/10.1063/5.0231002

We have demonstrated a complementary metal-oxide-semiconductor inverter logic gate by heterogeneous integration of an enhancement-mode n-channel transistor on GaN and a p-channel transistor on diamond. A thermally grown p-type NiOx is used as the dielectric, and Ni/Au is the gate metal for both transistors. NiOx oxide on top of a partially recessed-gate AlGaN/GaN heterostructure depletes the two-dimensional electron gas by pulling the Fermi level closer to the valence band and making it normally OFF. The combination of Ni/NiOx gate metal work function and the dielectric helps to deplete the two-dimensional hole gas channel of a hydrogen-terminated p-channel diamond, making it an enhancement mode. The GaN n-MOS and diamond p-MOS transistors show output and transfer characteristics with threshold voltages of +0.6 and −1.2 V, respectively. nMOS and pMOS transistors show ION/IOFF current ratios of >105 and >103, respectively, with a subthreshold leakage of <10 μA/mm. The gate current is negligible for both devices. The saturation drain current of the respective transistors is measured to be ∼170 and ∼20 mA/mm at a gate-to-source overdrive voltage of 3 V. The inverter input–output characteristics and transient response are measured for various rail-to-rail voltages and frequencies. The inverter threshold voltage is measured to be 1.1 V for a nominal operating voltage of 3 V.

High mobility p-channel GaN heterostructures grown by MOCVD through impurity engineering

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The p-GaN/AlGaN/GaN heterostructures with integrated n-channel and p-channel have been extensively applied in p-channel field effect transistor (p-FET) devices and complementary (CMOS) logic circuits. However, the hole mobility of the p-channel is still low, especially in the heterostructures grown by metalorganic chemical vapor deposition (MOCVD). In this work, an impurity engineering was designed by introducing Ga vacancies in the p-channel, so that the diffused Mg impurity could substitute the Ga site and form MgGa−1 rather than Mginter+2. The charged impurity scattering was hence suppressed due to the reduction of the impurity charge. As a result, the GaN heterostructure with a hole mobility of 21.8 cm2/V·s with a sheet hole density of 1.02 × 1013/cm2 was realized at room temperature by MOCVD. This work paves a way for improving the transport properties of GaN heterostructures and lays a foundation of high performance GaN-based p-FET devices and CMOS logic circuits on Si substrates.

Comprehensive study of Schottky-gated p-channel GaN field-effect transistors

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Appl. Phys. Lett.
https://doi.org/10.1063/5.0245557

In this work, a comprehensive study of Schottky-gated p-channel GaN field-effect transistors (GaN PFETs) with an energy-band modulated AlGaN barrier layer, a variable gate structure, and various densities of holes in the p-GaN layer is demonstrated to optimize electrical performance. The design rules for high-performance Schottky-gated GaN PFETs not only offer diverse pathways to achieve enhancement-mode operation but also improve output current density. Based on the design rules, a high-performance enhancement-mode GaN PFET with a high ION/IOFF ratio of 3 × 106, a low SS of 130 mV/dec, and a negative VTH of −1.09 V is fabricated, which is conducive to promoting the development of the low-power GaN complementary metal–oxide–semiconductor driving circuits.

Enhancing thermal dissipation ability and electrical performance in GaN-on-GaN HEMTs through stepped-carbon buffer design

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This study investigates the thermal dissipation ability and electrical performance of GaN-on-GaN HEMTs through a stepped-C buffer design. We analyzed the relationship between impurity (C and Fe) concentrations and the thermal conductivity of the GaN material by fitting Debye–Callaway model. A stepped-C buffer design is proposed to avoid the Fe impurity and its tailing effect on thermal conduction in GaN epitaxial layers. In addition, the high concentration of C doping is designed to suppress the epitaxial interface leakage in GaN-on-GaN structures. The transducer-less transient thermoreflectance (TL-TTR) technique revealed that the stepped-C structure significantly improves thermal conductivity of epitaxial layers compared with that of Fe/C co-doped structure. Due to the optimization of heat dissipation ability, the peak temperature of the stepped-C sample decreased by ∼30 °C compared to the Fe/C co-doped sample at PDC = 10.4 W/mm. Consequently, the GaN-on-GaN HEMTs with the stepped-C buffer achieved a record output power density (Pout) of 14.8 W/mm and a power-added efficiency (PAE) of 48.2% at 3.6 GHz, underscoring the critical role of thermal management in advancing GaN-on-GaN HEMT RF performance.

A surface potential analysis method and I–V model of AlGaN/GaN high-electron mobility transistors incorporating the two lowest subbands

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An analysis method for the surface potential model and current–voltage model of AlGaN/GaN high-electron mobility transistors (HEMTs) is proposed. In this paper, the two lowest subbands E0 and E1 in the triangular electron potential well are incorporated into this model, which can preferably reflect the electronic structure and carrier transport mechanism of HEMTs. Then, the proposed method of compound-proximity algorithm overcomes the bottleneck of the compromise between the accuracy and efficiency of GaN HEMTs' physics-based model. Additionally, the self-heating effect is introduced into the current model, which can effectively reflect the degradation of output characteristics caused by the increase in the device temperature. The results of numerical simulations, experiments, and our model are compared across a wide range of operating regimes for HEMTs to demonstrate the validity of AlGaN/GaN HEMTs' modeling. This modeling method offers a fresh research approach for AlGaN/GaN HEMT modeling and paves a novel path toward overcoming the technical hurdles in advanced process integrated

circuit design associated with Electronic Design Automation tools.

(Ultra)wide bandgap semiconductor heterostructures for electronics cooling

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Appl. Phys. Rev.
https://doi.org/10.1063/5.0185305

The evolution of power and radiofrequency electronics enters a new era with (ultra)wide bandgap semiconductors such as GaN, SiC, and β-Ga2O3, driving significant advancements across various technologies. The elevated breakdown voltage and minimal on-resistance result in size-compact and energy-efficient devices. However, effective thermal management poses a critical challenge, particularly when pushing devices to operate at their electronic limits for maximum output power. To address these thermal hurdles, comprehensive studies into thermal conduction within semiconductor heterostructures are essential. This review offers a comprehensive overview of recent progress in (ultra)wide bandgap semiconductor heterostructures dedicated to electronics cooling and are structured into four sections. Part 1 summarizes the material growth and thermal properties of (ultra)wide bandgap semiconductor heterostructures. Part 2 discusses heterogeneous integration techniques and thermal boundary conductance (TBC) of the bonded interfaces. Part 3 focuses on the research of TBC, including the progress in thermal characterization, experimental and theoretical enhancement, and the fundamental understanding of TBC. Parts 4 shifts the focus to electronic devices, presenting research on the cooling effects of these heterostructures through simulations and experiments. Finally, this review also identifies objectives, challenges, and potential avenues for future research. It aims to drive progress in electronics cooling through novel materials development, innovative integration techniques, new device designs, and advanced thermal characterization. Addressing these challenges and fostering continued progress hold the promise of realizing high-performance, high output power, and highly reliable electronics operating at the electronic limits.

Self-aligned fabrication of vertical, fin-based structures

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J. Vac. Sci. Technol. B
https://doi.org/10.1116/6.0004047

Modern power devices rely on complex, three-dimensional, vertical designs to increase their power density, ease their thermal management, and improve their reliability. However, fabrication techniques have historically relied on 2D processes for patterning lateral features. This work presents a new technology that uses multiple steps of angled depositions to fabricate self-aligned vertical, fin-based devices that avoid fundamental lithography resolution and alignment limitations. The fabrication flows of two devices, the self-aligned vertical finFET and the high-κ dielectric fin diode, are presented to demonstrate how angled depositions can readily achieve transistors with submicrometer, vertical gates in a source-first process and also create high-aspect ratio GaN fins with a record 70:1 aspect ratio.

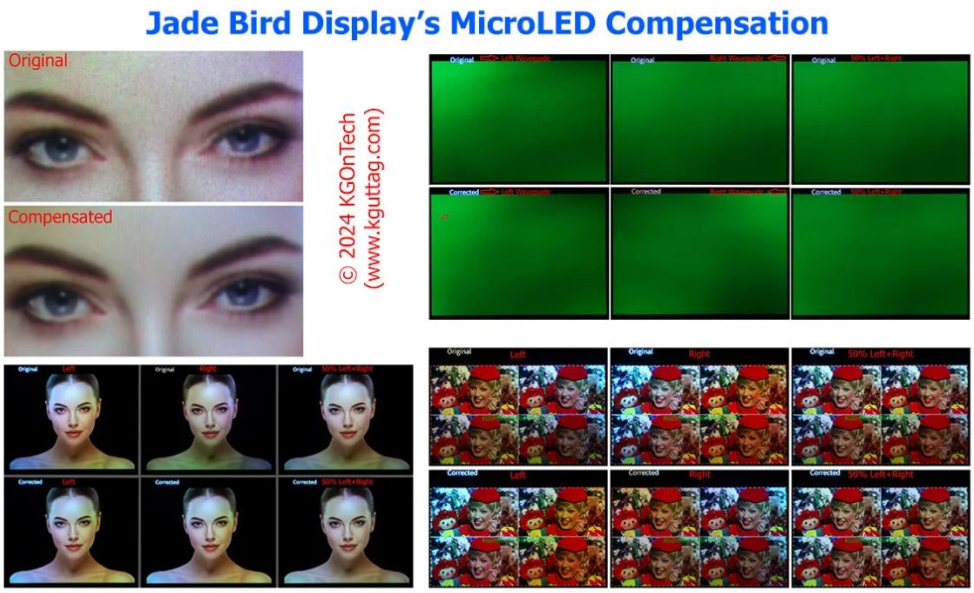
PRESS RELEASES

Technical and economic information selected by Knowmade

OPTOELECTRONICS

Jade Bird Display's MicroLED Compensation

LedInside



Introduction

At SID Display Week in May 2024, MicroLED maker Jade Bird Display (JBD) had a large booth that showed their devices, a number of customer systems, and a "compensation demo." JBD offered to loan me their compensation demo. After sending me one of the demos from SID and my taking many pictures to evaluate it, JBD informed me that they would be able to send me a newer demo in a couple of months, so I decided to wait for the newer system before reporting my results. Between the availability of the systems and my travel, many months have passed.

This article starts with quite a bit of "background information," which I think is helpful in understanding the results. Perhaps the most controversial issue is that JBD says their compensation is based on both eyes. I felt the need to add some information on "Binocular Rivalry," which discusses how human vision responds to seeing different content in each eye. Human vision is complex, to say the least, and while I think what JBD claims is mostly true, it oversimplifies what people see.

All images in JBD's demo were pre-loaded into the demo system. JBD's current devices have a more limited real-time correction built into the display and controller. The stills in the demo were pre-processed to demonstrate what will be possible in real-time with their new chipset. JBD allowed me to submit a series of test patterns that they added to their set of demo images, which I appreciate. Still, I couldn't try any new test patterns based on my findings (which I often do with other headsets when I see an effect that I want to investigate further).

I should also note that the demo systems did not have the full heat-sinking capability that would be incorporated into a product. This limited the number of bright pixels, particularly red ones, that could be shown in a single image.

JBD Dominates in MicroLED-Based AR Glasses

JBD is the only company I know of that is shipping MicroLEDs, and the only ones I have seen in any headset product or even prototype. At the same time, Meta CTO Andrew Bosworth stated in videos that Meta "designed" Orion's MicroLEDs, and it is most likely that Jade Bird Display is making Orion's MicroLEDs. It has been widely rumored that Meta's 2020 MicroLED deal with Plessey fell apart (example: https://www.microled-info.com/meta-announces-10000-ar-glasses-powered-microled-microdisplays), and there are no other likely suspects. Perhaps Meta got a change in resolution to make it a custom part. It appears Meta "designed" the MicroLEDs in a similar way that Apple "designed" the Micro-OLEDs used in the Apple Vision Pro when it is known that Sony manufactured the Micro-OLEDs for Apple.

PlayNitride has demonstrated a full-color MicroLED display using blue MicroLEDs with Quantum dot red and green color conversion with a Lumus Waveguide (but not in a headset) at AR/VR/MR 2023 (see MicroLEDs with Waveguides (CES & AR/VR/MR 2023 Pt. 7)). PlayNitride has continued advancing its efforts with quantum dot color conversion MicroLEDs. Still, I have yet to see a headset.

JBD's booth featured AR glasses from multiple companies, including TCL's Ray New X2 (full-color 3-chip X-cube) Ray Neo X2 and several monochrome (green) AR glasses, including Vuzix Z100, LAWK's Meta Lens, MyVu AR, and INMO's Go. I have also seen JBD MicroLED-based monochrome AR glasses from Oppo and, more recently, Even Realities announced their small form factor AR glasses Even Realities G1: Minimalist AR Glasses with Integrated Prescription Lenses.

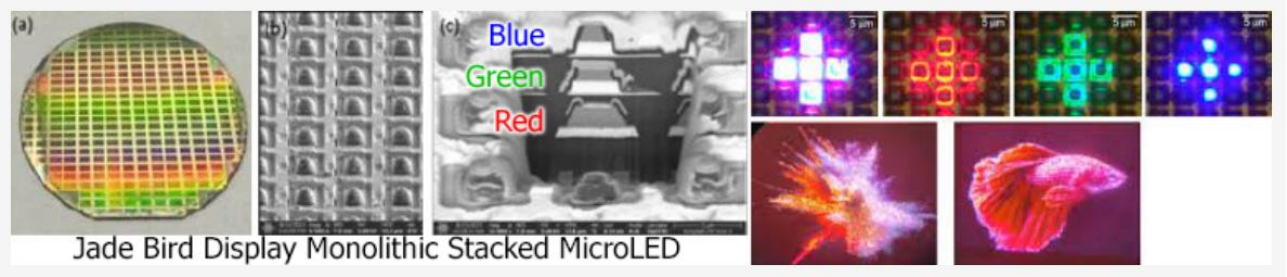
JBD's Current and Future Lineup

All the JBD MicroLED-based AR glasses to date use its monochrome 640×480 MicroLEDs with a 4-micron pixel. JBD offers projector optics for both single devices and has gone through a few generations of 3-Chip with X-Cube color combiners. JBD has been talking about 1280×720 monochrome devices with 5-micron pixels and monochrome 1920×1080 devices with 2.5-micron pixels for a few years, and JBD states that they plan on shipping devices to headset companies with 2.5-micron pixels for use in prototypes in 2025. JBD sells MicroLED panels, both with and without the optics, as shown below.

As I have discussed before, including in TCL and JBD X-Cube Color and our recent AR Roundtable Video Part 2: Meta Orion Technology and Application Issues, combining three monochrome panels to form a full-color image is a challenging alignment problem that is costly to manufacture. Most laymen will think about the horizontal and vertical alignment. Still, the more complex problem is aligning the panels in all dimensions, or the individual colors will not be in focus across the image. I think everyone in the industry believes that some form of "monolithic" approach will be required in the long run for MicroLEDs to be used in high volumes. I discussed the most well-known approaches to single-chip-full-color MicroLEDs in MicroLEDs with Waveguides (CES & AR/VR/MR 2023 Pt. 7). Among those approaches is the "stacked LED" method, which grows the various Red, Green, and Blue LED crystal layers on top of each other.

JBD Single Chip

JBD has developed and is sampling a stacked pixel device, but I have not personally seen it running. Unlike others that make the red, green, and blue LEDs all in variously doped Indium gallium nitride, JBD uses AlInGaN for the blue and green LEDs and AlInGaP for red. While red can be made in InGaN, it is generally not very efficient and high-yielding, whereas AlInGaP is more "natural" when making red. JBD is demonstrating that they have the process capability to mix the two types of LED crystal layers.



It's not clear when the stack LED approach will be better than the 3-chip method, at least for the immediate future. Perfecting the manufacturing of the complex process will likely take some time. The stacked approach limits the emission area of all three LEDs, and light from the lower layers will be blocked/lost by the upper layers. Then, there is the major issue of heat being trapped by the middle layers and LEDs heating each other. I discussed the various approaches to making full color with MicroLEDs in MicroLEDs with Waveguides (CES & AR/VR/MR 2023 Pt. 7), and each approach has its advantages and issues.

Read more

Graded Barriers Bandwidth Boost for Micro-LEDs on Silicon

LedInside

South China University of Technology and Guangdong Choicore Optoelectronics Company Ltd in China report on using graded indium gallium nitride (InGaN) quantum barriers (QBs) in blue light-emitting diode (LED) to improve the modulation frequency performance of devices grown on silicon (Si) with a view to deployment in visible light communication (VLC) systems [Lei Lei et al, IEEE Electron Device Letters, published online 11 November 2024].

The team sees VLC as a potential supplement to the overcrowded spectrum of existing wireless communication systems. "However, the lack of LED performance severely limits the development of VLC," the researchers point out.

VLC could be used in systems aimed at short-range positioning data exchange, indoor internet, etc. Such systems can be integrated into existing lighting infrastructure. Normal-size LEDs tend to have relatively low modulation bandwidths in the tens of MHz range. This can be improved by reducing the size of the LEDs. One drawback is that the smaller devices have lower light output power (LOP), impacting the signal to noise ratio.

One of the blockages to improving the frequency performance of InGaN LEDs is the built-in electric fields that arise from charge polarization contrasts of the III-nitride device layers. These fields tend to reduce the radiative efficiency due to the field pulling apart the electrons and holes that need to combine to emit photons.

By grading the InGaN barriers the researchers hoped to screen these fields, improving both bandwidth and LOP performance.

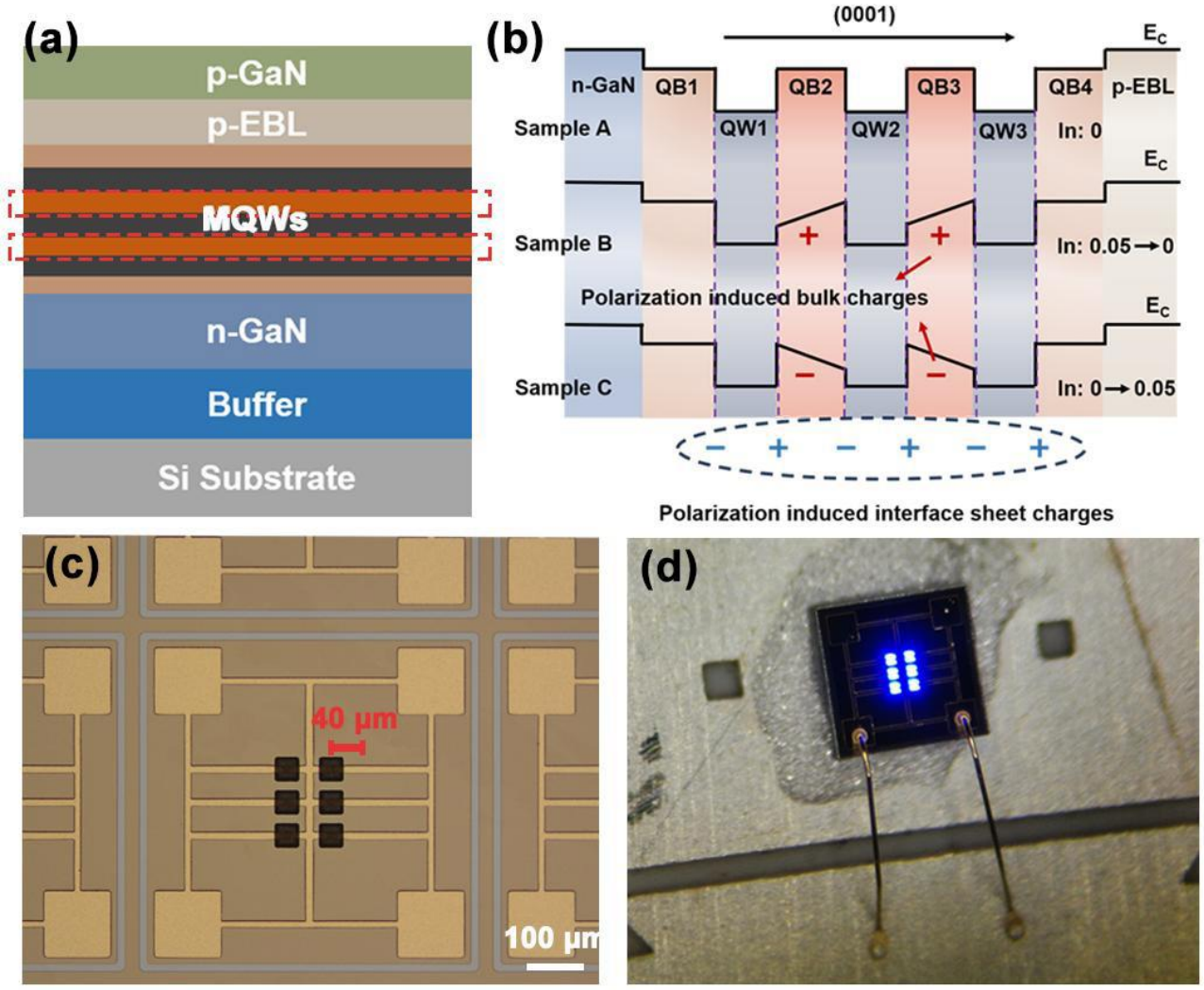


Figure 1: Schematic diagrams: (a) Si-substrate GaN-based LED epitaxial structure, and (b) conduction band for three samples. (c) Optical microscope image of sample, and (d) image of sample C operating at 10A/cm2.

The epitaxial structures used included 3µm n-GaN contact, 3x(3nm/4nm) In0.16Ga0.84N/InxGa1−xN multiple quantum well (MQW), 30nm p-type aluminium gallium nitride electron-blocking layer (EBL), and 60nm p-GaN contact layers (Figure 1). Three samples were processed with different InxGa1−xN profiles in the QBs: sample A had conventional pure GaN in the QBs 1–4 (i.e. x=0); sample B had the middle two QBs, 2 and 3, linearly graded from 5% to 0% along the (0001) growth direction, with the outer barriers pure GaN; and, sample C had the QBs graded in the opposite sense, from 0% to 5%.

According to simulations, the effect of the grading in sample C was to elevate the height of the triangular deep potential well between the last QB and the EBL, while diminishing the height of the valence-band barrier.

The team comments: “Such alterations are conducive to enhancing hole injection efficiency and mitigating electron escape, achieving a simultaneous increase in bandwidth and LOP of samples.”

The epitaxial material was fabricated into 2x3 arrays of micro-LEDs flipped onto a silicon conductive circuit substrate and bonded with gold/tin (Au/Sn). The micro-LEDs included a silver (Ag) reflector on the p-contact layer. The individual micro-LED units measured 40µmx40µm. The n-GaN contact layer was wired in parallel with sputtered titanium/aluminium/platinum/gold (Ti/Al/Pt/Au).

The devices needed slightly different forwardvoltage biases to give 1000A/cm2 current injection: 3.46V for sample A, and 3.44 and 3.41V for B and C, respectively.

The team comments: “Sample A has the highest voltage, potentially because of the higher series resistance and lower crystal quality. Moreover, the weaker polarization field in sample C decreases the height of triangle barrier of the valence band that the carriers need to overcome to inject into the MQWs, and thus the forward voltage.”

Sample C also showed 11% improvement over A in terms of light output power (LOP) — 28.9mW, compared with 26.1mW at 2000A/cm2. Array B had a LOP of 26.7mW at the same current injection point.

The peak wavelength shifted to shorter wavelengths in moving from low to medium current injection: 22nm in sample A, 19.1nm for B, and 17.9nm for C. The peak wavelength at the lowest current was around 450nm (~5nm higher for A, and ~5nm lower for C) The smaller shifts in B and C was attributed to the InGaN grading, and for C the favorable charge polarization configuration in the barriers. The external quantum efficiency for sample C was also improved by 10% over that of sample A (~5%) at 2000A/cm2.

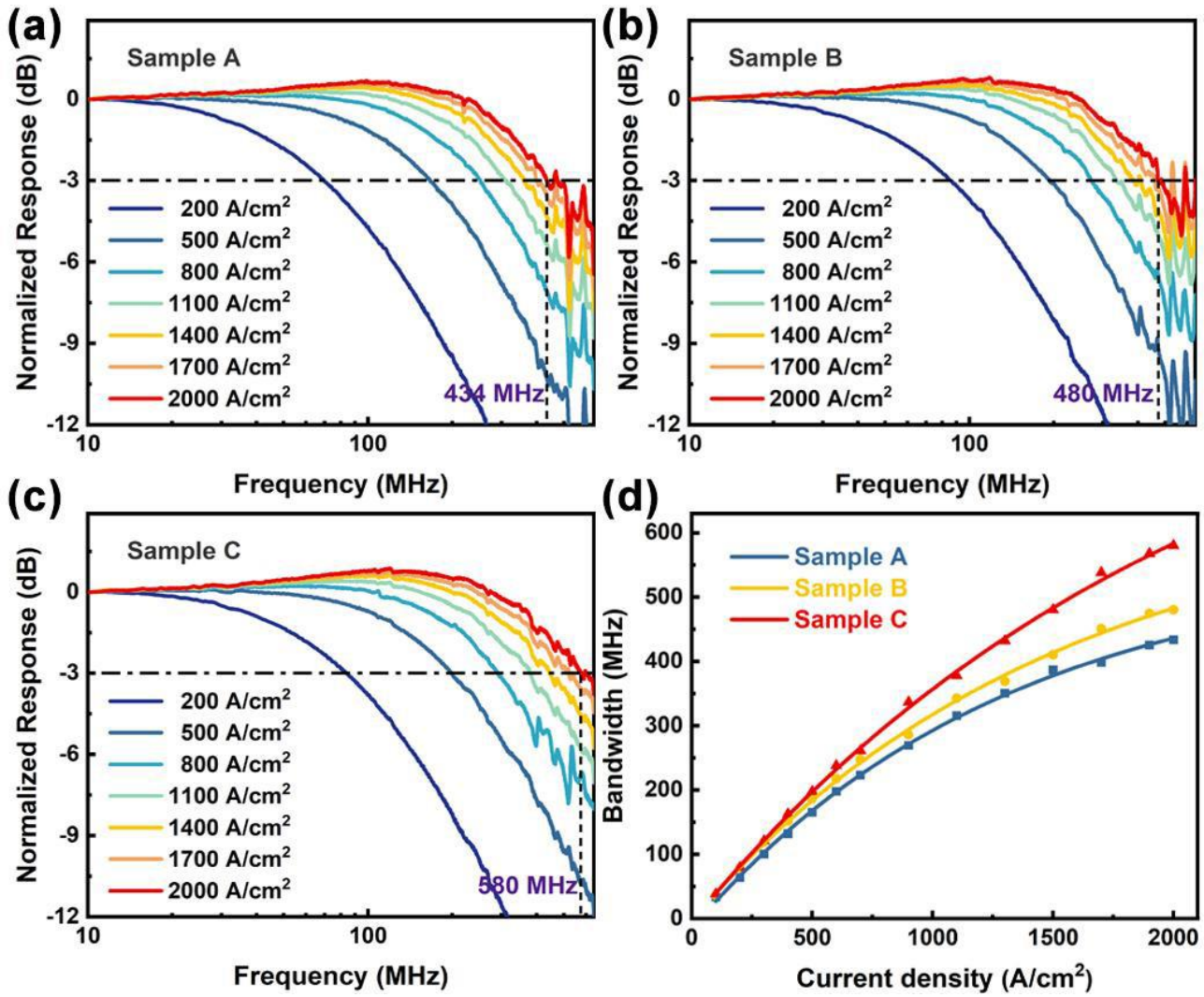


Figure 2: (a)-(c) Frequency responses of samples A–C under different current densities. (d) −3dB bandwidth versus current density.

Sample C also demonstrated a higher −3dB bandwidth — 580MHz at 2000A/cm2, compared with 434MHz and 480MHz for samples A and B, respectively (Figure 2).

The researchers comment: “The enhancement in −3dB bandwidth could be due to the weaker polarized electric field, which favors accelerated carrier radiative recombination. Concurrently, the lowered triangle barrier of the valence band causes an increase in hole concentration within the active region, thereby further enhancing the radiative recombination coefficient B.”

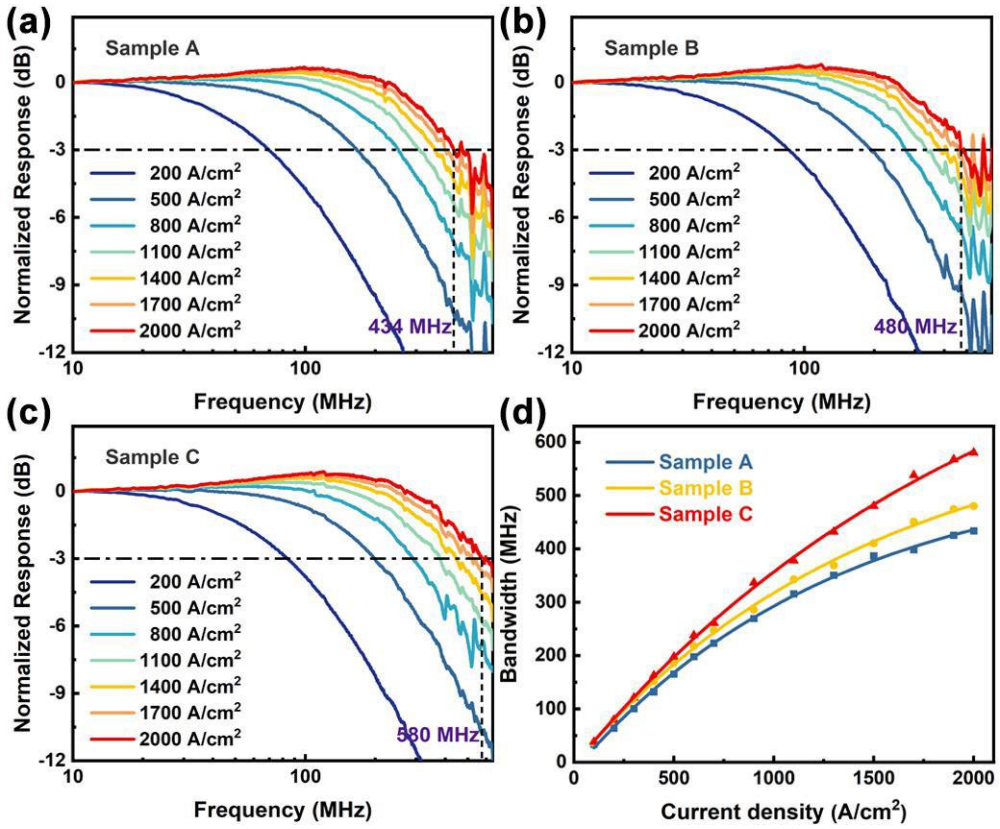


Figure 3: Comparison of −3dB bandwidth for micro-LED arrays with previous reports.

Comparing the bandwidth with previous research shows the South China/Guangdong sample C devices to have performance comparable to those grown on sapphire: high bandwidth at lower injection current density, compared with reports of LEDs on silicon.

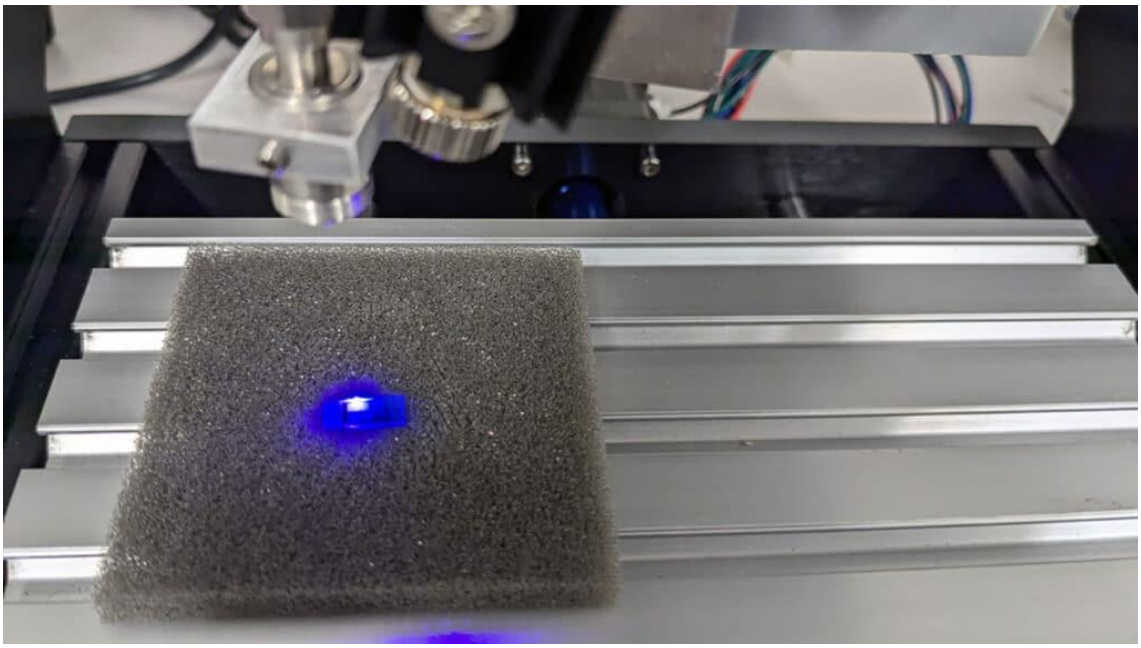
New way to make LEDs brighter and more efficient

LedInside

名古屋大学 NAGOYA UNIVERSITY Light-emitting diodes (LEDs) are everywhere in modern life, powering everything from smartphones to home lighting solutions. However, the current generation of LEDs has a significant drawback – when we increase their power for added brightness, efficiency takes a hit.

Now, a team of researchers at Nagoya University in Japan has introduced an innovative approach that promises to make LEDs brighter while maintaining their efficiency. Their research aims to reduce the cost and environmental

impact of LED production while improving performance in applications such as visible light communication and virtual reality (VR) glasses.



“The innovation of this work is a better understanding of the effects of polarization, an intrinsic property of the gallium nitride/indium gallium nitride (GaN/InGaN) layer structure that is needed for light generation,” lead researcher Markus Pristovsek said.

InGaN LEDs are considered the world’s most efficient source of light, although they generally function at low power levels. To achieve greater brightness, it is essential to raise their power. However, increasing the power supplied to the LED leads to a reduction in efficiency, a phenomenon referred to as efficiency droop.

To overcome this hurdle, expanding the LED area can result in more light output. However, this also requires a larger chip, leading to fewer LEDs being produced from a single wafer – the thin, flat semiconductor base made of InGaN used to fabricate LED devices. The outcome is higher manufacturing costs and a larger environmental footprint.

Researchers are actively working on mitigating efficiency droop by tilting InGaN layers and adjusting the wafer orientations, which significantly alters the crystal properties. One crucial property affected by this technique is ‘polarization.’ Although tilted orientations with low polarization have been under study for over 15 years, InGaN LEDs produced with these angles have consistently demonstrated less than 50% efficiency compared to standard high-polarization LEDs.

A study conducted by Pristovsek and Nan Hu at the Center for Integrated Research of Future Electronics (CIRFE) at Nagoya University revealed that lower polarization is advantageous only when it aligns with the orientation of standard LEDs. Building on this insight, the researchers grew LEDs on an economical sapphire substrate in the (10-13) orientation, which features reduced polarization while maintaining a direction akin to conventional LEDs.

These (10-13) LEDs demonstrate improved efficiency at higher power levels. This discovery indicates new possibilities for manufacturers to create advanced LED technologies, such as more efficient and brighter micro-LED screens for mobile devices and large televisions. Increased current density capacity could also lead to novel

applications in automotive and specialized industrial lighting, while quicker switching speeds could be useful in visible-light communication technology and VR eyewear.

“Future research is unlikely to find a better orientation, particularly on the cost-efficient sapphire substrates, because only two tilted directions can be fit to it,” Pristovsek said. “However, there are other ways to make (10-13) LEDs with fewer defects on sapphire and maybe even silicon. But the other orientations achieved on sapphire or silicon so far are worse because they are either inherently rough, they increase the amount of polarization, or they have the wrong sign of polarization.”

Why Micro-LED Defines the Future of AR Glasses

LedInside

SHENZHEN, China, Dec. 6, 2024 /PRNewswire/ -- VRTUOLUO, a new media platform focused on the VR/AR industry, has conducted an in-depth analysis of the AR glasses industry, shedding light on the technological advancements that are shaping its future. Here is the full article:

Tech giants are in a race to shape the future of innovation, with augmented reality (AR) glasses at the forefront of this technological revolution. Among the latest developments, Meta's introduction of "Orion"—a pioneering AR glasses prototype—stands out as a significant step toward transforming AR into an everyday computing platform.

Meta's Orion: Setting New Standards for AR

For many, the mention of AR glasses may bring back memories of Google Glass in 2012 or the subsequent evolution of devices like HoloLens and Magic Leap. Meta's Orion, unveiled at the Meta Connect event, epitomizes a pivotal leap in the realm of AR technology, merging cutting-edge performance with a lightweight design that reimagines the potential of AR glasses.

The announcement generated significant media attention and propelled Meta's market value soaring to a record market cap of $1.51 trillion in early October. This surge reflects not just enthusiasm for Orion but also growing investor confidence in AR technologies as a key driver of future innovation. Developers on Meta's platforms are excited about the prospect of creating content for Orion, indicating a growing momentum towards the convergence of AR and VR technologies.

Industry leaders also had high praise for Orion. Nvidia founder Jensen Huang described Orion's display as exceptional[1], while former Google executive Hugo Barra likened the experience to trying autonomous driving technology for the first time—an acknowledgment of AR's transformative potential[2].

Although Orion is currently available only to developers, Meta is already looking ahead to commercialization, aiming for broader availability within three years. This milestone underscores Meta's outsized influence in shaping the trajectory of XR technologies and serves as a critical benchmark for the entire industry.

Pioneering AR with Lightweight Micro-LED Technology

One of Orion's distinguishing characteristics is its lightweight design, made possible by Micro-LED displays and silicon carbide waveguides. For AR glasses, portability and comfort are essential requirements—cumbersome form factors impede widespread adoption.

Micro-LED technology is revolutionizing AR display capabilities with its ultra-compact and lightweight design. The industry's smallest Micro-LED projector measures just 0.15 cubic centimeters, weighing only 0.3 grams—small enough to fit seamlessly into the temple of a pair of glasses. This breakthrough enables AR glasses to resemble everyday eyewear, moving away from bulky goggles or helmet-like designs.

Outdoor AR requires in-eye brightness levels of at least 2,000 to 3,000 nits. Micro-LED polychrome waveguide modules, however, deliver an impressive 6,000 nits—far exceeding this threshold. In addition to its exceptional brightness, Micro-LED offers superior energy efficiency thanks to pixel-level independent light control, making it significantly more power-efficient under equivalent conditions. When considering brightness, power consumption, contrast ratio, and lifespan, Micro-LED outperforms alternatives like LCoS and DLP, making it the clear choice for next-generation AR devices.

Meta's choice of silicon carbide for its waveguides further enhances Orion's capabilities. With a refractive index of 2.6, silicon carbide avoid optical artifacts like rainbow and leakage enables a wider field of view while offering excellent thermal stability and durability. Though expensive, the material has spurred industry-wide investment, with competitors now exploring similar designs to replicate Orion's success.

The impact of Orion's debut is undeniable. Rumors surrounding Apple's "Atlas" smart glasses project and reports of Samsung's accelerated AR efforts indicate that the race to dominate the AR market is intensifying. The next generation of AR glasses is shaping up to be lightweight, powerful, and feature-packed.

Micro-LED: The Future of AR Displays

Meta's reliance on Micro-LED reflects a broader industry trend: global brands are adopting this technology for AR glasses. In the past year, devices like DreamSmart's StarV Air 2, OPPO's Air Glass 3, and Even Realities' G1 have debuted slim, stylish designs, with some models weighing under 40 grams. These innovations highlight a shared vision across the industry: creating AR glasses that are practical, lightweight, and suitable for all-day wear.

The exceptional performance of Micro-LED technology has drawn significant attention from both tech giants and innovative startups in recent years. Companies like Apple, which acquired Micro-LED pioneer LuxVue as early as 2014, and industry leaders such as Meta, Snap, Samsung, and LG, have been building robust patent portfolios in this space. According to Yole Group, global Micro-LED patent filings have surged exponentially, with over 11,000 new patents published through the 2021-2023 period.[3]

The adoption of Micro-LED technology is reshaping the AR landscape, enabling a new generation of lightweight, wearable devices. At the forefront of this innovation is JBD, a leader in Micro-LED microdisplays and the sole company currently engaged in their mass production. JBD's displays now power over 25 AR glasses models globally, marking a significant leap toward transforming AR from bulky headsets to streamlined, everyday wearables.

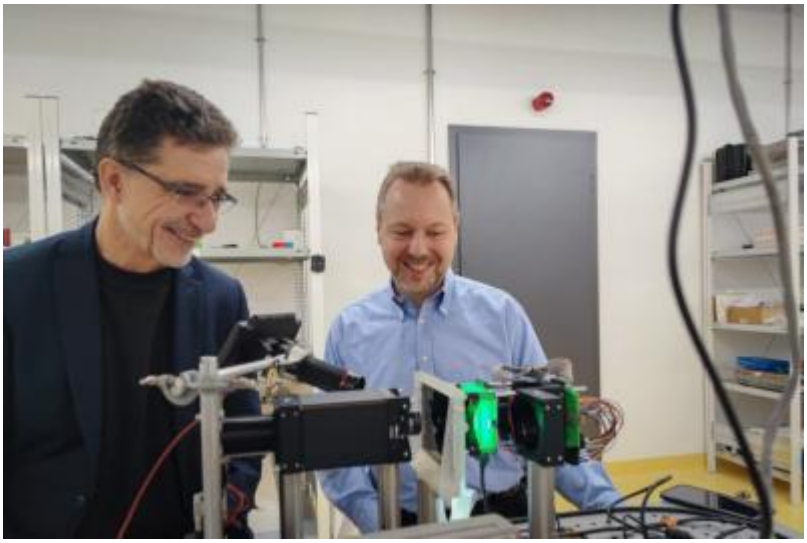
As AR glasses are poised to become the next major computing platform, driven by AI-powered contextual computing, JBD's new strategy, "JBD Enlightened," positions the company as a key catalyst for the AR revolution. Similar to how "Powered by Android" became a hallmark of the smartphone era, JBD aims to become synonymous with next-generation displays powering immersive AR experiences.

Meta CEO Mark Zuckerberg envisions a future where glasses become the main way we do computing, with smartphones gradually taking a backseat.[4] With Orion's debut, this vision feels closer than ever, marking the dawn of a transformative era for AR technology.

TU Braunschweig researchers, in collaboration with OUAS and ams-OSRAM are looking into using microLEDs for AI computing

LedInside

Researchers at the Nitride Technology Centre (NTC) at TU Braunschweig, in collaboration with Ostfalia University of Applied Sciences and ams OSRAM, are looking into the use of microLED devices in neuromorphic computing. The researchers say that the adoption of microLED devices may lead to highly efficiency AI computers.



The basic idea is to mimic the biological neural network by using photonic components. The researchers are combining GaN components with conventional silicon microelectronics to create highly integrated arrays with hundreds of thousands of micro-LED. Using microLEDs can enable a power reduction by a factor of 10,000 compared to current technologies.

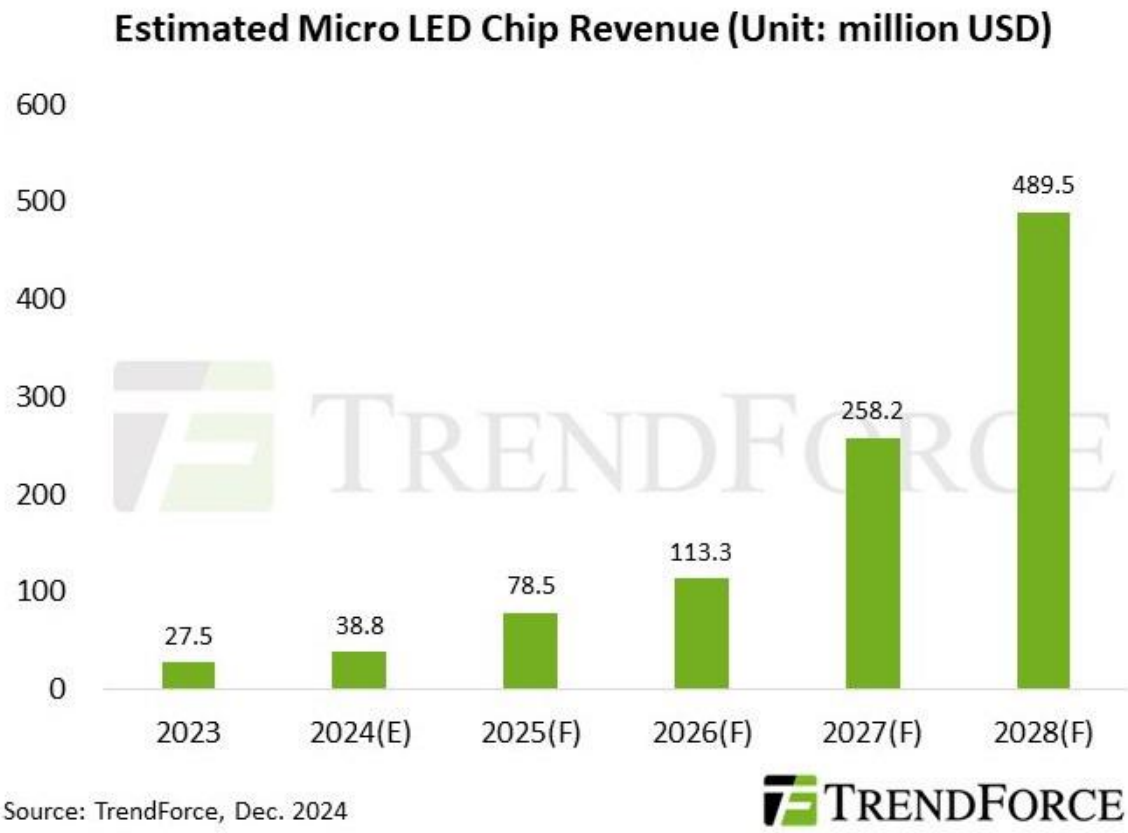
This is still early research, but the researchers have already developed a macroscopic optical micro-LED demonstrator with 1,000 neurons, that has passed a standard AI pattern recognition test.

Micro-LED chip market to grow from $38.8m in 2024 to $489.5m by 2028

SemiconductorToday

Revenue from micro-LED chips will reach about $38.8m in 2024, with large displays remaining the primary contributor, forecasts market research firm TrendForce. Looking ahead, breakthroughs in technical bottlenecks are on the horizon, while applications in automotive displays and the increasing maturity of full-color augmented-reality (AR) glasses solutions are expected to drive the micro-LED chip market to $489.5m by 2028.

TrendForce highlights several challenges confronting the micro-LED industry in 2024. First, the slow progress in chip miniaturization has hindered cost-reduction efforts. Second, the high price of micro-LED displays has resulted in weak end-user demand, limiting the shipments of large-sized displays already in production. Third, the focus in the wearable device market has shifted to software optimization and hardware–software integration. This has reduced the incentive for brands to innovate hardware and slowed the adoption of new display technologies like micro-LEDs. Lastly, while automotive applications remain a key area of promise for micro-LEDs, they are still in the early stages of adoption and validation, making it difficult to contribute significantly to revenue in the short term.



From a technical perspective, addressing the challenge of seamless large-sized display assembly is crucial. In the short term, improving backplane production yield through different driving schemes can enhance efficiency and reduce costs. Over the medium to long term, increasing backplane size to minimize the number of required assemblies could eliminate complex manufacturing steps such as side wiring and TGV (through-glass vias).

Additionally, maximizing light extraction efficiency is becoming increasingly important in micro-LED display design and production. Techniques such as microstructure and reflective structure design can reduce light loss and improve brightness by optimizing reflected light.

TrendForce points out that, as the yield rate of mass transfer technology improves, new challenges are emerging in inspection processes. Although the LED industry already has established testing methods, these solutions require refinement to handle the extreme miniaturization and high volume of micro-LED chips. Addressing these inspection challenges is currently a critical priority for the industry.

The micro-LED's standout characteristics — high brightness, high contrast, and high transparency — continue to attract investment from manufacturers. These features enable micro-LED to integrate into transparent displays for automotive windows or as part of AR-HUD or P-HUD systems, meeting the growing demand for seamless integration of virtual- and real-world information for drivers and passengers. Additionally, combining micro-LEDs

with silicon substrates offers a robust solution for near-eye displays in AR glasses, positioning micro-LEDs as a benchmark for next-generation metaverse-focused head-mounted devices.

TrendForce emphasizes that the commercialization of micro-LED technology should not depend overly on the mature consumer electronics market. Instead, manufacturers should capitalize on the unique capabilities of micro-LEDs for displays, pairing them with diverse sensor solutions to empower devices with new functionalities and uncover imaginative niche applications. This strategy is expected to accelerate the penetration of micro-LEDs across various markets, further driving growth and innovation.

NUBURU resolves non-compliance with NYSE rules

SemiconductorToday

NUBURU Inc of Centennial, CO, USA — which was founded in 2015 and develops and manufactures high-power industrial blue lasers — says that NYSE Regulation has sent it a warning letter, as provided under Section 1009(a) of the NYSE American LLC Company Guide, describing violations by the firm of Sections 301 and 713 of the Company Guide.

Section 301 prohibits a listed company from issuing, or authorizing its transfer agent or registrar to issue or register, additional securities of a listed class until it has filed an application for the listing of such additional securities and received notification from the NYSE American that the securities have been approved for listing.

Section 713 requires stockholder approval when additional shares to be issued in connection with a transaction involve the sale, issuance or potential issuance of common stock (or securities convertible into common stock) equal to 20% or more of outstanding stock for less than the greater of book or market value of the stock.

As noted in the letter, NUBURU issued about 4.6 million common shares between May and August in connection with the conversion of certain convertible promissory notes that NYSE has determined were in violation of these provisions. NUBURU says that it is consequently implementing additional controls to avoid violations of such NYSE rules in the future.

Aledia at CES 2025: Shaping the Future of Display Technology

Aledia

Aledia is happy to participate in the CES 2025 in Las Vegas! From January 7th to 10th, visit us at the Venetian Expo, Hall G – 60711, Eureka Park, Booth 04 located within the Auvergne Rhône-Alpes region pavilion.

This year, we are showcasing our groundbreaking microLED technologies, including:

- D-LED (Digital LED) A high-performance miniLED solution for local dimming backlighting units in LCDs.
- NOVA High Voltage microLED Based on 3D nanowires, seamlessly integrated onto TFT backplanes.
- Single Color and RGB Microdisplays: Designed to optimize power efficiency and form factor.

Our innovations drive next-generation displays across a range of applications, from automotive displays (CID and HUD) to augmented and virtual reality, smartphones, laptops, and televisions.

We are also highlighting our new 15 000 m² manufacturing facility in Champagnier, a key milestone in building Europe's "Display Valley" and establishing a robust local production ecosystem for microLEDs.

We look forward to welcoming you at CES 2025 and sharing how Aledia's technology can shape the future of displays.

VueReal Highlights Revolutionary MicroLED Solutions at CES 2025

VueReal

Waterloo, Ontario – December 12, 2024 – VueReal, a pioneer in MicroSolid Printing technology, is excited to showcase its latest innovations for consumer electronics at CES 2025, January 7-10, in Las Vegas. These cutting-edge advancements are poised to redefine the future of displays and human-machine interfaces (HMI) for various devices, including TVs, tablets, IT displays, smartwatches, smartphones, automotive, and more.

Leveraging its proprietary MicroSolid Printing™ platform, VueReal delivers breakthrough microLED solutions that address key challenges in the consumer electronics space, such as transparency, power efficiency, and enhanced HMI capabilities. With these technologies, VueReal is driving the next wave of consumer product innovation—faster, more efficiently, and at a reduced cost.

In addition, VueReal will unveil its industry-first Design Reference Kits, marking the first time the industry has been equipped with comprehensive tools to accelerate the adoption of microLED technology. These kits are designed to streamline product development across multiple sectors, from automotive and augmented reality (AR) to

medical devices, lighting, and beyond, helping companies bring their microLED-driven products to market faster and more cost-effectively.

Key Innovations to be Highlighted at CES 2025

- Cost-Competitive Transparent Displays: VueReal makes transparent displays accessible for mainstream consumer applications. From ultra-thin, high-brightness TVs and IT monitors to sleek tablets and mobile devices, VueReal's transparent microLED displays combine striking aesthetics with exceptional energy efficiency, offering immersive, next-gen viewing experiences. The company's QuantumVue™ Display technology further enhances these capabilities, providing a path to producing mid- to large-size microLED displays with superior performance at costs competitive with today's OLED solutions.
- Power-Generating Displays: VueReal transforms portable electronics with revolutionary power-generating microLED displays. Integrating solar harvesting capabilities, these displays enable devices like smartwatches and smartphones to extend battery life by converting ambient light into usable energy. This innovation promotes sustainability and enhances the user experience by reducing the need for frequent charging.
- Advanced Human-Machine Interfaces (HMI): VueReal's microLED-based solutions drive advancements in HMI technology, delivering ultra-high-resolution, energy-efficient displays, and interactive touch interfaces for current and emerging consumer hardware. Whether in gaming, productivity tools, or smart home systems, VueReal's solutions elevate device functionality while improving user experience.
- High Transparency Laminated Displays: VueReal will showcase its cutting-edge high-transparency laminated displays in 3.5" and 10” sizes. These displays offer unprecedented clarity and seamless integration capabilities, making them ideal for automotive windshields, smart home appliances, and next-generation mobile devices. The laminated design ensures durability and versatility, opening up new possibilities for embedded displays in everyday objects.

"Our advanced microLED solutions for consumer electronics, powered by our MicroSolid Printing platform, aren't just about improving displays—they're about creating entirely new possibilities for everyday devices," said Dr. Reza Chaji, CEO of VueReal. "From transparent TVs to energy-efficient smartwatches, our technology is designed to empower manufacturers to deliver the next wave of innovative, user-centric products."

Why Visit VueReal at CES 2025?

- Live Demonstrations: Experience VueReal's transparent displays, power-generating screens, HMI solutions, and Design Reference Kits firsthand and see how they can transform consumer electronics and accelerate product development.
- Expert Collaboration: Discuss your product concepts with VueReal's team and discover how our microLED technology and Developer Kits can accelerate your product development process.
- Future-Ready Solutions: Explore how VueReal's platform supports sustainable, scalable, high-impact innovations that will shape the consumer electronics industry.

CrayoNano AS Launches HE-Series UV-C LED: High-Performance Disinfection Technology for Water, Air, and Surfaces

Crayonano

Trondheim, Norway—CrayoNano AS proudly announces the next evolution in our CrayoLED UV-C LED product family—the HE-series UV-C LED, CLH1-N3S. Designed to meet the growing global demand for reliable, price-effective, and sustainable UV disinfection solutions, the HE-series delivers high power, excellent efficiency, and product reliability for water, air, and surface disinfection applications.

"After two years of market experience and collaborating on over 150 design-in projects, we've seen a clear demand from customers for improved price-performance ratios in large-scale, high-volume disinfection applications," said Michael Peil, CRO at CrayoNano. "The HE-series is our answer—a product that delivers the right balance of quality, performance, germicidal power, and price-efficiency. It faciliates customers to scale their solutions competitively, enabling development of next level, demanding high-power applications and unlocking access to new market segments and opportunities."

Key Features and Benefits of the HE-Series (CLH1-N3S):

- High Germicidal Power: Optimized packaging technology delivers improved chip efficiency of > 5%, achieving stable output of 150 mW at 500 mA, enabling maximized deactivation against harmful pathogens.
- Exceptional Durability: Built on CrayoNano's proven H-series platform, the HE-series maintains over 90% of its UV-C power output after 1,000 hours of operation under rigorous accelerated testing conditions of Wet High Temperature Operating Life (WHTOL, 90 % relative humidity and 60 °C ambient environment temperature, Iv = 350 mA, Tj =~82 °C), translating to an L70 lifetime of 15,000 hours at nominal driving currents.
- Advanced Thermal Management: Featuring a 15% reduction in thermal resistance compared to previous models, the HE-series ensures reliable, consistent, and long-lasting performance.
- Flexible System Integration: Operable at higher driving currents for diverse applications, the HE-series offers system design versatility for municipal water treatment, food processing, HVAC systems, agriculture, and industrial curing disinfection applications.
- Performance to Price-Effective and Eco-Friendly: The HE-series is engineered for performance to price ratio (PPR), delivering over a 30% improvement over its lifetime. These benefits extend to UV systems integrating the HE-series UV-C LEDs, offering an energy-efficient, low-maintenance, and mercury-free disinfection solution. This reduces environmental impact while optimizing total cost of ownership (TCO) and enabling faster returns on investment (ROI) for businesses.

Why Choose the HE-Series UV-C LED?

The HE-series reflects CrayoNano's commitment to sustainability and innovation in UV-C disinfection by delivering UV-C LED components that prioritize efficiency and sustainability, meeting the evolving needs of our customers and the industry. We are excited to announce the planned addition of a 265 nm product line to the CrayoLED HE-series, set to launch in Q2 2025. This new offering expands our portfolio, providing customers with a broader optimization range to meet their specific application requirements. Complementing the existing 275 nm product

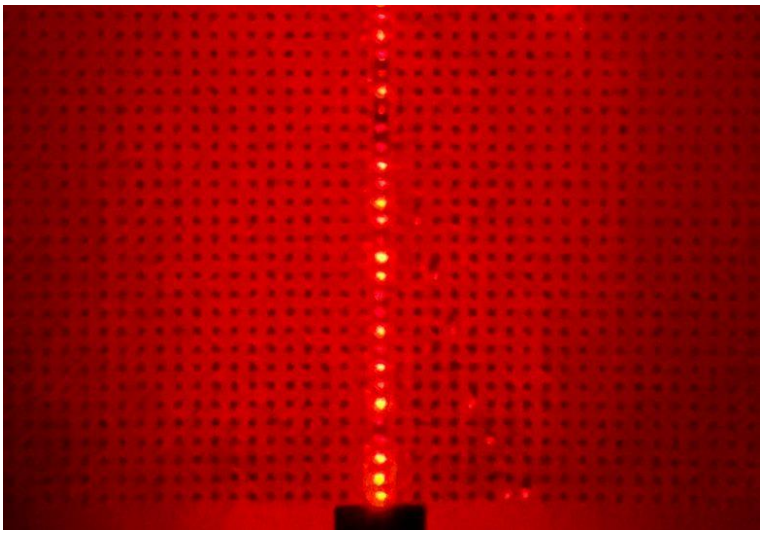
line, the 265 nm upholds CrayoNano's values for quality and disinfection performance, delivering the reliability and price-effectiveness our customers need for high quality, affordable, and scalable solutions, this next-generation LED enalbes our customesr to meet disinfection demands effectively and sustainably.

Breakthrough in microLED development: Red pyramidal microLED based on the same material as green and blue

Polar Light Technologies

Linköping, Sweden, 2024-12-18

In a remarkable breakthrough in their research, Polar Light Technologies has achieved red light of 625 nm based on the company's non-etching bottom-up concept. This means Polar Light Technologies have reached red, green, and blue pyramidal microLEDs using the same material compound.



The pyramidal design has the ability to be manufacturable while maintaining excellent microLED performance, laying the foundation for monolithic RGB displays.

This milestone marks the culmination of years of rigorous research and development, truly enabling spatial computing and next-generation panel displays.

Red without compromise

Blue and green MicroLEDs have been in the market for years, but reaching a red colour has been difficult due to fundamental challenges in the material properties. There are several workarounds or alternatives for reaching a red colour, but they all come with some compromises, such as efficiency, manufacturability, or the need to integrate with other material systems.

“Pursuing Polar Lights’ innovative pyramidal LED concept has been about overcoming those challenges without compromises. Today, thanks to a great tech team, we have succeeded in realizing the red-emitting microLEDs based on our innovative pyramidal structure”, says Lisa Rullik, CTO of Polar Light Technologies.

Unique pyramidal structures

Polar Light Technologies’ microLED is composed of pyramid shapes that are built with a novel bottom-up approach, a technology that comes with unique benefits:

The inevitable strain in the lattice-mismatched InGaN/GaN structures is reduced, which is important to be able to manufacture blue, green, and red microLEDs with the same material system, that is, to build monolithic RGB.

It gives a unique possibility to integrate the frontplane with a backplane

No etching is needed, which means:

- Performance is maintained also for smaller dimensions since no etching damages occur
- Enables even sub-µm LEDs – nanoLEDs
- Easier to manufacture and integrate with CMOS and TFT
- Narrow emission cone: Lambertian light lobe from the emitter, which is important for microprojectors

With these unique benefits, the microLED from Polar Light Technologies solves key challenges in bringing the technology to the market.

Performance, manufacturability and nanoLED

Polar Light Technologies’ same-compound-based microLED offers high performance and excellent manufacturability. Its very small dimensions and narrow emission cone further enhance the offer. The technology also opens up for nanoLED applications – as soon as the rest of the display technology catches up.

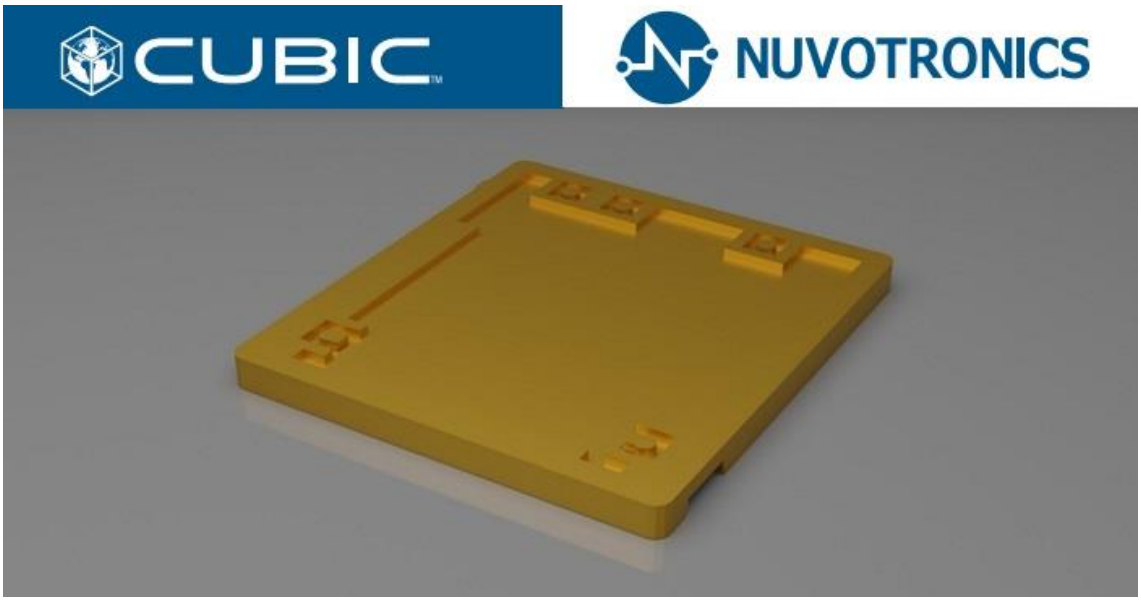
“Our technology addresses microLED challenges in a way that has never been done before,” says Oskar Fajerson, CEO of Polar Light Technologies. “Now we’re moving towards commercialization of this groundbreaking technology, focusing on putting products on the market.”

ELECTRONICS

Nuvotronics Uses PolyStrata® Technology to Develop High-Performance Package for Qorvo's GaN Amplifiers

everything RF

Nuvotronics, a division of Cubic Mission & Performance Solutions, has introduced the PolyStrata® Package (PSP1029439), an innovative packaging solution designed for Qorvo's TGA2962 2-20 GHz 10-Watt GaN Amplifier. The new package enhances thermal management, stability, and ease of integration while maintaining the amplifier's optimal performance, making it ideal for high-demand applications in military, space, communications, and instrumentation.



Key Features and Benefits

The PSP1029439 package offers advanced capabilities tailored for modern engineering challenges. Its efficient heat dissipation system removes thermal reliance on the PCB by channeling heat through the package lid and sides. Additionally, its compact dimensions of 5.5 x 6 x 1.45 mm and SMT compatibility simplify integration into standard processes, while built-in wire-bonded capacitors improve stability.

This solution ensures ease of use with a robust design that is compatible with automated gold wire bonding and standard solder reflow processes. Its immersion gold-over-immersion silver surface finish further enhances its reliability in diverse environments.

Optimized Thermal Management

Nuvotronics conducted extensive thermal analysis, demonstrating the PSP1029439's ability to handle significant heat dissipation efficiently. Removing heat via the package lid, for instance, reduces case temperatures compared to traditional PCB-based cooling, leading to improved performance under high-power conditions.

For example, using silver sinter paste as an adhesive and maintaining the heat sink at 25°C results in a channel temperature of 195°C at 45W power dissipation, underscoring the package's capability to sustain heavy loads.

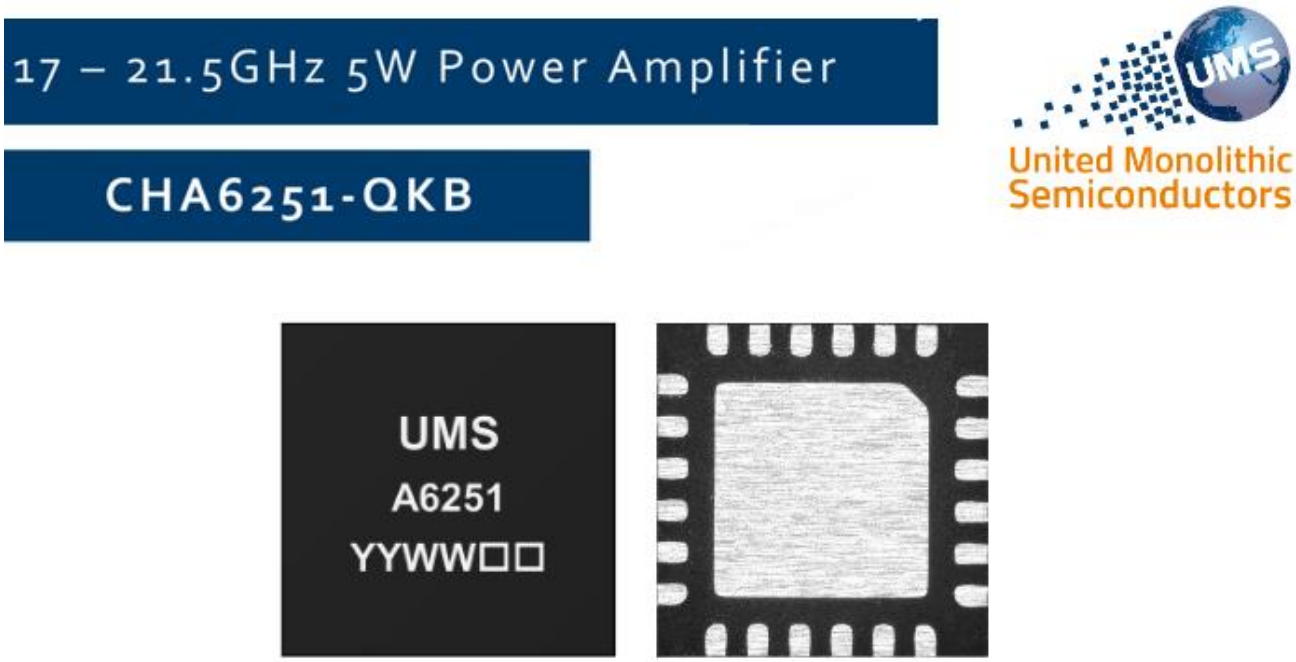
Broad Applicability

The PSP1029439 package is ideally suited for critical sectors such as military and space, where durability and reliability are paramount. It is also effective in high-frequency communication and instrumentation systems, offering enhanced performance and operational stability across various domains. Click here for more information on PSP1029439.

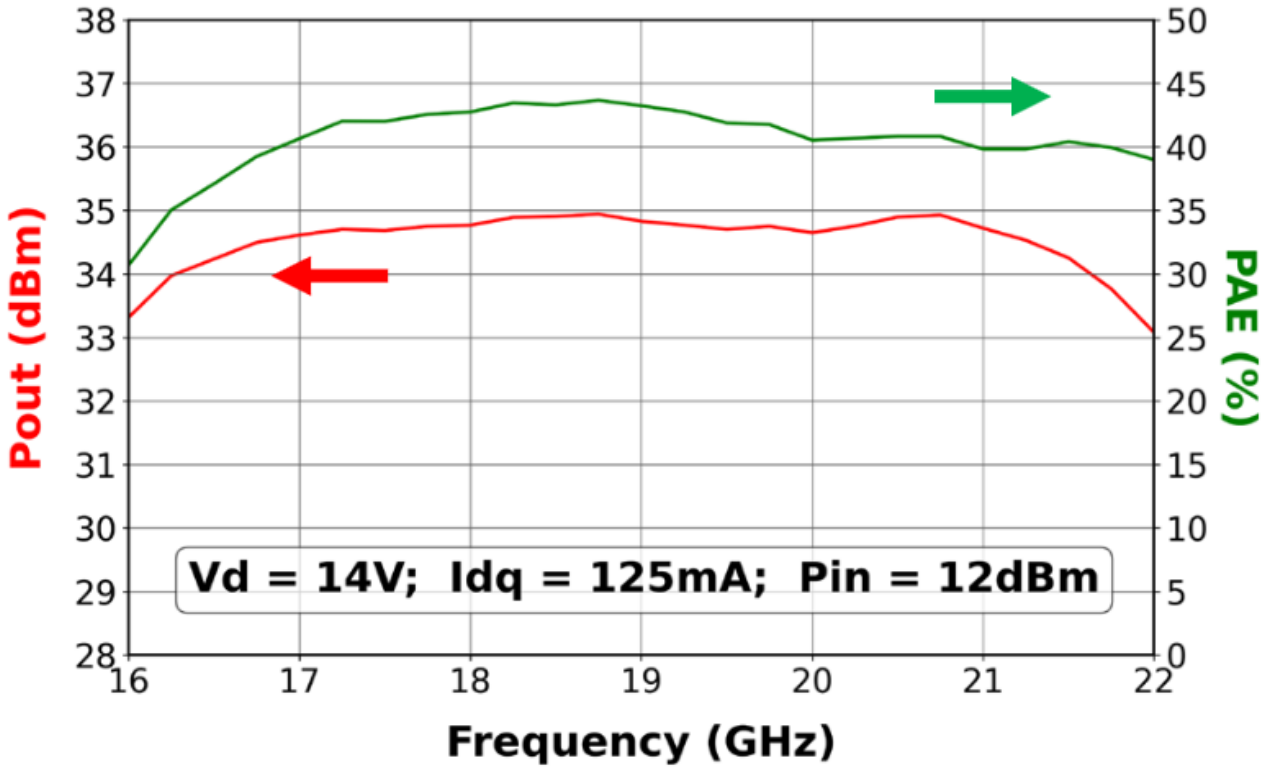
United Monolithic Semiconductors Introduces 5 W GaN-on-SiC Power Amplifier from 17 to 21.5 GHz

everything RF

United Monolithic Semiconductors (UMS) has introduced the CHA6251-QKB, a three-stage power amplifier that operates in the frequency range from 17 to 21.5 GHz. It can deliver output power anywhere between 33 dBm to 37 dBm depending on the bias point with a linear gain of more than 30 dB and a power-added efficiency (PAE) of 42%. The CHA6251-QKB is manufactured using robust GaN-on-SiC HEMT process incorporating monolithic technology. This amplifier requires a DC supply of 14 V and consumes 125 mA of current. It is available in a 24-lead surface-mount QFN package that measures 4 x 4 mm. This power amplifier is RoHS-compliant and is rated to moisture sensitivity level 3 (MSL3) standard.



This amplifier has been designed primarily for space applications but it can also be used in a wide array of microwave systems. It is also provided with an evaluation board that is compatible with the proposed footprint, and uses a microstrip to coplanar transition to access the package for testing purposes.



Advantages and Applications of GaN Push-Pull Amplifiers

Microwave Journal

Gallium Nitride (GaN) has emerged as the preferred high-power amplifier (HPA) technology due to its superior properties compared to LDMOS technology. GaN enables wider bandwidth and higher efficiency amplifier designs, allowing a single wideband amplifier to replace multiple narrowband amplifiers. This reduces board space without sacrificing performance. While a wideband amplifier design offers advantages in terms of space and cost, its broad bandwidth presents challenges in meeting harmonics requirements.

Push-pull power amplifier (PA) topology is gaining popularity as the architecture of choice for many applications like land mobile radios (LMR) and tactical radios. This topology combines two or more PAs to achieve higher power output, resulting in improved efficiency, lower distortion and reduced power dissipation. This also simplifies thermal management challenges.

This article discusses various wideband GaN amplifier topologies and demonstrates why push-pull topology is the ideal solution for optimal performance in wideband PA designs. It compares the pros and cons of a HPA design using two push-pull PAs combined with a 90-degree hybrid versus two PAs combined with baluns. Additionally, the article addresses the specific requirements of low-power and high-power LMR handsets in terms of efficiency, distortion, power handling and thermal management. The article explains how push-pull amplifiers can reduce overall system size while maintaining these critical parameters. It will also present measured performances of recent designs of low-power and high-power push-pull amplifiers that use existing PAs from TagoreTech to address the challenges faced in LMR handset applications.

HPA TECHNOLOGIES

GaN and LDMOS are two of the most common semiconductor process technologies for PA design. With an ever-increasing demand to reduce the size, weight, power and cost (SWaP-C), GaN is rapidly replacing LDMOS in many

new PA designs. This is, in part, because LDMOS transistors are typically built on a silicon substrate, while some advanced designs may use silicon-on-insulator substrates.

Due to its material properties, GaN offers several advantages over silicon. Table 1 highlights the basic material properties of both GaN and silicon. The properties listed in Table 1 show that GaN devices have much higher power density due to a higher breakdown voltage, saturation velocity and charge density. This higher power density enables GaN devices to be significantly smaller for the same output power, reducing all device capacitances compared to existing LDMOS technology. Lower input and output capacitances facilitate the realization of broadband matching networks. Additionally, higher voltage operation increases the load line impedance for a desired output power, further aiding in the realization of broadband output matching. These factors make GaN an excellent choice for PAs, RF components and functions in other demanding electronic systems where performance and reliability are critical.

TABLE 1

COMPARISON OF GAN AND SILICON TECHNOLOGY

Property	GaN	Silicon
Energy Band Gap (eV)	3.4	1.1
Critical Electric Field (MV/cm)	3 to 4	0.3
Charge Density	Higher	Lower
Thermal Conductivity (W/cm·K)	1.3 to 1.5	1.5 to 1.6
Electron Mobility ($cm^2/V·s$)	1000 to 2000	1400
Thermal Stability	High	Moderate
Saturation Velocity (cm/s)	2×10^7	1×10^7
Breakdown Voltage	High	Moderate
Cost of Fabrication	Higher for SiC substrate Moderate for silicon substrate	Lower due to mature technology

BROADBAND PA TOPOLOGIES AND TRADE-OFFS

Broadband PAs are essential components across a wide range of applications, enabling effective communication, enhancing signal quality and ensuring reliability in various fields, from telecommunications to consumer electronics and beyond. The performance of these PAs enables them to handle a broad frequency range, making them versatile components in modern communication systems. Several broadband PA topologies are available, each with its advantages and disadvantages. Some important topologies include:

- **Lossy Matched Amplifier or Multistage Lumped Element Matching**: This topology employs multistage input and output matching networks with lumped elements like resistors, capacitors and inductors to achieve wider bandwidth.
- **Feedback Amplifier**: Negative feedback is applied to extend the bandwidth. Both shunt and series feedback configurations have been used in this context, but shunt feedback generally yields the best results.

- **Distributed Amplifiers**: This topology uses the concept of "additive amplification" with multiple transistors and offers ultra-broadband operation that can extend from DC up to the cutoff frequency of the active devices.
- **Push-Pull Amplifiers**: A push-pull amplifier configuration uses two active devices to address the positive and negative cycles of an input signal. This design improves efficiency and reduces distortion by canceling even-order harmonics, making it particularly effective in audio and RF applications. By alternating the conduction between the two devices, push-pull amplifiers can deliver high output power while maintaining good linearity and thermal performance. Complementary operation, reduced distortion and improved thermal stability contribute to the overall bandwidth improvement of push-pull amplifiers.

Table 2 summarizes the comparison of different broadband PA topologies. Distributed amplifiers typically offer the maximum bandwidth among the four types of PA topologies listed. This makes them suitable for applications requiring very wide frequency coverage. Push-pull amplifiers and feedback amplifiers can also provide extended bandwidth but generally do not reach the same levels of bandwidth as distributed amplifiers.

TABLE 2

COMPARISON OF BROADBAND AMPLIFIER TOPOLOGIES

Topology	*Bandwidth*	*Efficiency*	*Linearity*	*Design Complexity*
Lossy Matched Amplifier	Moderate	Low	Moderate	High
Feedback Amplifier	Moderate	Moderate	High	Moderate
Distributed Amplifiers	High	High	Moderate	High
Push-Pull Amplifiers	Moderate to High	High	High	Moderate to High

When considering distortion, efficiency and other factors like bandwidth, both push-pull and distributed amplifiers have their strengths. However, push-pull amplifiers stand out in terms of efficiency, ease of design, reduced distortion, better heat management and lower costs. This makes them an excellent option for high-power applications, such as tactical radio and LMR systems.

GaN push-pull PAs have distinct advantages over other technologies due to the properties of GaN. This amplifier topology/technology choice delivers better efficiency, wider bandwidth, higher power density and improved thermal performance. Overall, these benefits make GaN push-pull amplifiers an appealing option for various applications, including telecommunications, aerospace and defense systems.

PUSH-PULL DESIGN APPROACH

The push-pull design approach uses two transistor or HEMT-based devices to amplify an input signal. In this setup, one device handles the positive half of the waveform while the other manages the negative half. Figure 1 shows the basic building block of a push-pull PA.

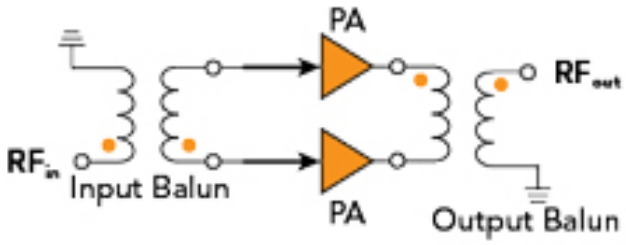


Figure 1 Push-pull PA block diagram.

The push-pull design approach uses two transistor or HEMT-based devices to amplify an input signal. In this setup, one device handles the positive half of the waveform while the other manages the negative half. Figure 1 shows the basic building block of a push-pull PA.

The key components of a push-pull PA are:

- **Input Stage**: The input signal is typically differential, coming from a source that can produce balanced outputs. A balun converts the single-ended unbalanced signal into two equal but opposite phase-balanced signals that drive the two active devices.
- **Active Devices**: Two active FETs or HEMTs are arranged in a push-pull configuration. Each device handles one half of the input waveform. One amplifies the positive half, while the other amplifies the negative half.
- **Balun**: A balun is located at the input and output of the PA. At the input, the balun translates the single-ended signal into a differential signal. At the output, it translates the differential signal back into a single-ended signal. The balun can also be designed to provide impedance transformation for the desired bandwidth. It helps in minimizing common-mode noise and ensures that the power is evenly distributed between the two devices.
- **Output Stage**: The outputs of the two transistors are combined at the output stage. The balun ensures that the combined output is in phase and delivers the amplified signal to the load.
- **Feedback Mechanism (optional)**: Feedback can be implemented to improve linearity and reduce distortion. It may be applied from the output back to the input stage, stabilizing the overall gain.

The input signal enters the amplifier, where the balun converts it into two balanced signals. The two active devices amplify their respective halves of the signal. The amplified outputs are fed into the balun, which combines them into a single unbalanced output. The output is delivered to the load (e.g., an antenna), providing high power with low distortion. The architecture of a push-pull PA using a balun effectively combines the benefits of balanced operation and push-pull design, resulting in high efficiency, low distortion and broader bandwidth.

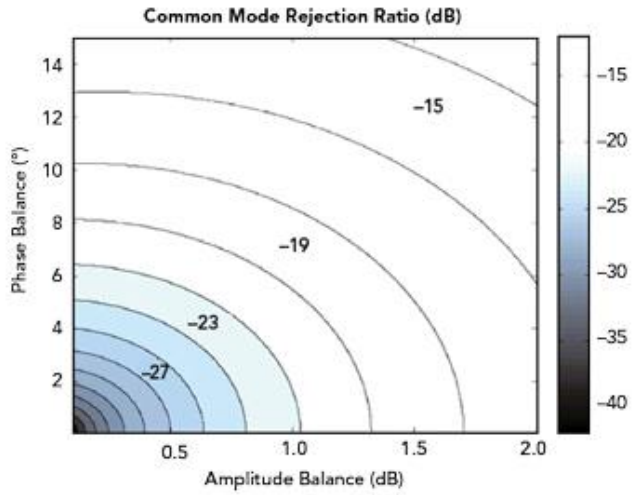
CRITICAL BALUN PARAMETERS

The design/selection of the balun is one of the most critical factors in the design of push-pull PAs. Several factors need to be considered when designing or selecting the correct balun for the amplifier design:

- **Operational Bandwidth**: The bandwidth where the balun must meet the specified requirements.
- **Insertion Loss**: A critical parameter that directly impacts the overall efficiency of the amplifier. Higher insertion loss also limits the power handling capability of the balun and may make thermal management challenging.
- **Amplitude and Phase Imbalance**: Directly impacts the achievable common-mode rejection ratio (CMRR) of the balun.
- **Impedance Transformation Ratio**: The desired ratio between the input and output impedances.
- **Power Handling**: The maximum power the balun can handle without exceeding its specified limits.

A CMRR of 20 to 25 dB is commonly achievable in a balun over a wide bandwidth. Figure 2 shows a chart of CMRR versus phase and amplitude imbalance. This chart shows that a balun must have less than 0.5 dB of amplitude imbalance and 5 degrees of phase imbalance to achieve 25 dB CMRR. These imbalance values need to be measured at the even-order harmonic frequencies.

The maximum power requirements of the amplifier drive the maximum power handling requirements of the baluns. Higher power baluns that are used on the PA output will typically be larger due to thermal management considerations. This is a critical factor when designing baluns.



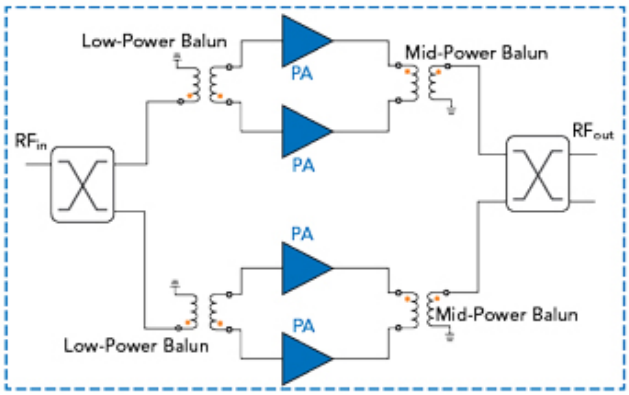


Figure 2 CMRR versus amplitude and phase imbalance. **Figure 3** Push-pull PA using hybrid 90° couplers.

Trending GaN Transistors in 2024

everythingPE

Gallium Nitride (GaN) transistors are advanced wide bandgap (WBG) semiconductors that offer higher efficiency, faster switching speeds, and lower losses compared to traditional silicon devices. With a wide bandgap of 3.4 eV, GaN enables operation at higher voltages, frequencies, and temperatures, allowing for compact, high-power density designs. These features make GaN transistors ideal for applications like electric vehicles, renewable energy

systems, wireless charging, and 5G telecommunications. In this article, everything PE has listed some interesting GaN Transistors that were trending on the website in 2024.

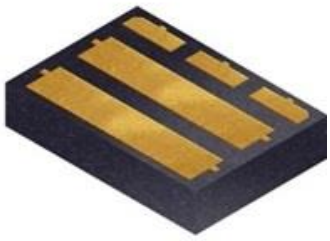
100 V Enhancement-Mode GaN Power Transistor

The EPC2361 from Efficient Power Conversion is an Enhancement Mode GaN Power Transistor that is ideal for synchronous rectification, DC-DC conversion, motor drives, and solar MPPT applications. It has a drain-to-source voltage of over 100 V, a gate threshold voltage of up to 2.5 V, and a drain-source on-resistance of less than 1 milli-ohm. It is available in a surface mount package that measures 3 x 5 mm. Read more.

50 V Enhancement Mode GaN-on-Si Power Transistor

The INN150LA070A from Innoscience is an Enhancement Mode GaN-on-Silicon Power Transistor. The transistor has a drain-source breakdown voltage of 150 V, a gate threshold voltage of 1.1 V, and a drain-source on-resistance of 7 milli-ohms. It is available in a surface-mount package that measures 3.2 x 2.2 mm and is ideal for synchronous rectification, class-D audio, high-frequency DC-DC converter, communication base station, and motor driver applications. Read more.

300 V Radiation Hard eGaN Power Transistor



The EPC7030G from EPC Space is a Radiation Hard eGaN Power Transistor that is ideal for commercial and industrial applications. This transistor has a drain-source voltage of over 300 V, a gate threshold voltage of 1.4 V, and a drain-source on-resistance of less than 32 milli-ohms. This MIL-STD-750-compliant power transistor is available in a surface-mount package. Read more.

650 V Direct Drive D-Mode Power Switch for Power Supply Applications

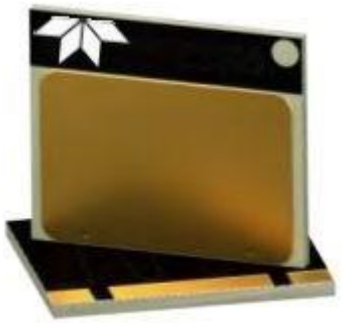
The V08TC065S1X11 from VisIC Technologies is a Direct Drive D-Mode Power Switch that has been designed for applications requiring high power and efficiency with low volume and cost. It has a drain-source voltage of 650 V, a gate-source voltage of over -25 V, and a drain-source on-resistance of 8 milli-ohms. It is available in a surface-mount package that measures 21 x 23 x 3 mm and is ideal for solar inverters, AC-DC power supplies, AC motors, laser drivers, battery chargers, and automotive applications. It is available in a surface-mount package that measures 21 x 23 x 3 mm and is ideal for solar inverters, AC-DC power supplies, AC motors, laser drivers, battery chargers, and automotive applications. Read more.

650 V Enhancement Mode GaN Power Transistor for Datacom Applications

The GAN140-650EBEZ from Nexperia is an Enhancement Mode GaN Power Transistor that is ideal for high power density and high-efficiency power conversion, AC-to-DC converters, totem pole PFC, DC-to-DC converters, fast battery charging, mobile phones, laptop, tablet and USB type-C chargers, datacom and telecom (AC-to-DC and DC-to-DC) converters, motor drives, solar (PV) inverters, Class D audio amplifiers, TV PSU and LED driver applications. This transistor has a drain-source voltage of up to 650 V, a gate threshold voltage of less than 1.7 V, and a drain-source on-resistance of 140 milli-ohms. This RoHS-compliant GaN transistor is available in a surface-mount package that measures 8 x 8 mm. Read more.

650 V Enhancement Mode GaN-on-Silicon Power Transistor

The TDG650E601TSP from Teledyne e2v HiRel Electronics is an Enhancement Mode GaN-on-Silicon Power Transistor that is ideal for battery management, traction drives, dc-dc converters, space motor drives, and bridgeless totem pole PFC applications. This GaN transistor has a drain-source voltage of up to 650 V, a gate threshold voltage of 1.7 V, and a drain-source on-resistance of 25 milli-ohms. It is available in a PCB-mount package that measures 9.00 x 7.64 mm. Read more.



600 V Enhancement Mode GaN Power Transistor for SMPS Application

The IGLR60R260D1 from Infineon Technologies is an Enhancement Mode GaN Power Transistor. This transistor has a drain-source voltage of up to 600 V, a gate threshold voltage of less than 1.6 V, and a drain-source on-resistance of 370 milli-ohms. It is available in a surface-mount package that measures 6 x 5 x 1.1 mm and is ideal for industrial and consumer SMPS (based on the half-bridge topology) applications. Read more.

1200 V N-channel GaN Power Transistor for Power Adapter Applications

The GPI120R12T74IC from GaNPower International is an N-channel GaN Power Transistor ideal for switching power, power adapters, and power delivery charger applications. This GaN transistor has a drain-source voltage of up to 1200 V and a drain-source on-resistance of less than 18 milli-ohms. This transistor is available in a through-hole package that measures 15.70 x 40.64 mm. Read more.

Enhancement Mode GaN Power Transistor for PV inverter Applications

The CGD65C025SP2 from Cambridge GaN Devices is an Enhancement Mode GaN Power Transistor that is ideal for industrial, datacentre and telecom SMPS, industrial motor drives, PV inverters, uninterruptible power supplies, and energy storage systems applications. This transistor has a drain-source voltage of up to 650 V, a gate-source voltage from -1 V to +20 V, and a drain-source on-resistance of 25 milli-ohms. This normally off-power GaN power transistor is available in a surface-mount package that measures 10 x 10 mm. Read more.

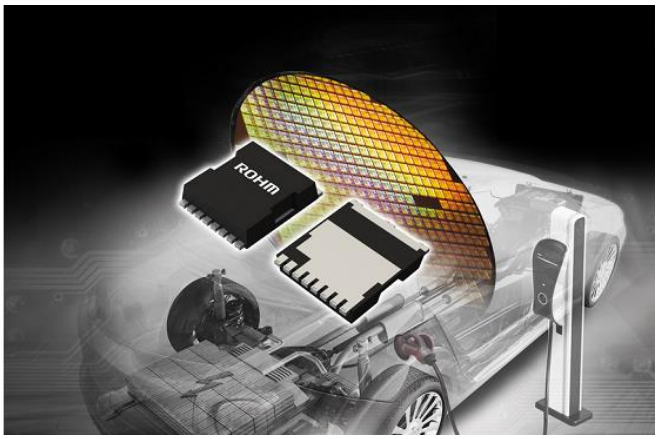
650 V GaN Field Effect Transistor for Datacom Applications

The TP65H070G4RS-TR from Transphorm is a GaN Field Effect Transistor that is ideal for datacom, broad industrial, PV inverter, servo motor, and computing applications. It has a drain-source breakdown voltage of over 650 V, a gate threshold voltage of 4 V, and a drain-source on-resistance of less than 85 milli-ohms. This RoHS-compliant GaN transistor is available in a surface-mount package that measures 9.26 x 10 mm. Read more.

ROHM and TSMC Collaborate on GaN Power Device Production for Evs

everythingPE

ROHM announced that ROHM and TSMC have entered a strategic partnership on the development and volume production of gallium nitride (GaN) power devices for electric vehicle applications. The partnership will integrate ROHM's device development technology with TSMC's industry-leading GaN-on-silicon process technology to meet the growing demand for superior high-voltage and high-frequency properties over silicon for power devices.



GaN power devices are currently used in consumer and industrial applications such as AC adapters and server power supplies. TSMC, a leader in sustainability and green manufacturing, supports GaN technology for its

potential environmental benefits in automotive applications, such as on-board chargers and inverters for electric vehicles (EVs).

The partnership builds on ROHM and TSMC's history of collaboration in GaN power devices. In 2023, ROHM adopted TSMC's 650 V GaN high-electron mobility transistors (HEMT), whose process is increasingly being used in consumer and industrial devices as part of ROHM's EcoGaN™ series, including the 45 W AC adapter (fast charger) "C4 Duo" produced by Innergie, a brand of Delta Electronics.

"GaN devices, capable of high-frequency operation, are highly anticipated for their contribution to miniaturization and energy savings, which can help achieve a decarbonized society. Reliable partners are crucial for implementing these innovations in society, and we are pleased to collaborate with TSMC, which possesses world-leading advanced manufacturing technology" said Katsumi Azuma, Member of the Board and Senior Managing Executive Officer at ROHM. "In addition to this partnership, by providing user-friendly GaN solutions that include control ICs to maximize GaN performance, we aim to promote the adoption of GaN in the automotive industry."

"As we move forward with the next generations of our GaN process technology, TSMC and ROHM are extending our partnership to the development and production of GaN power devices for automotive applications," said Chien-Hsin Lee, Senior Director of Specialty Technology Business Development at TSMC. "By combining TSMC's expertise in semiconductor manufacturing with ROHM's proficiency in power device design, we strive to push the boundaries of GaN technology and its implementation for EVs."

Astute Group Partners with Wise-integration for GaN Device Distribution

everythingPE

Astute Group, a leading global electronics distributor and supply-chain solutions provider, and Wise-integration, a French pioneer in digital control of gallium nitride (GaN) and GaN ICs for power conversion, announced a strategic distribution partnership covering Europe, the Middle East and Africa (EMEA).

Wise-integration's WiseGan family of GaN power devices and WiseWare digital control software deliver significant performance advantages over conventional silicon-based solutions, including superior efficiency, reduced footprint, and enhanced switching frequencies.

WiseGan includes GaN power integrated circuits designed for high-frequency operation in the MHz range, integrating features that streamline implementation with digital control. WiseWare is a 32-bit, MCU-based AC-DC digital controller optimized for GaN-based power-supply architectures.

"Wise-Integration's decision to partner with Astute speaks volumes about their strategic vision and commitment to market leadership," said Kevin Baker, Astute's Franchise Division Manager. "Their embedded systems, manufactured with TSMC's leading-edge technology, can be integrated into virtually any electronic component. Our collaboration empowers Astute's customers with the best GaN solutions available, ensuring they stay ahead in today's rapidly evolving technological landscape."

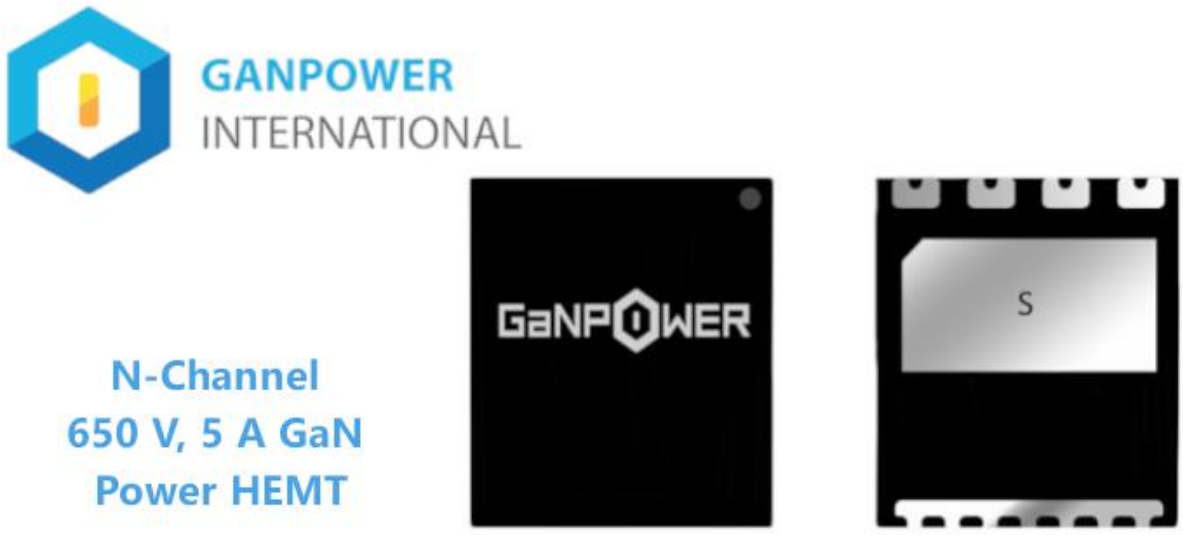
"Following the recent launch of our North American Design & Development Center in Canada and our Wise-integration subsidiary in Hong Kong, this partnership with Astute Group is a significant step in expanding the global reach of our digital GaN power solutions," said Wise-integration CEO Thierry Bouchet. "As a recognized leader in electronics distribution, Astute's extensive network and deep industry expertise will be invaluable in accelerating the adoption of GaN technology across key EMEA markets."

This collaboration is designed to drive significant innovation and accelerate the integration of GaN technology across a broad spectrum of sectors, including consumer electronics, electric vehicles, data centers, and industrial automation.

GaNPower Introduces N-Channel 650 V Power GaN HEMTs

everythingPE

GaNPower International has unveiled the GPI65005, a GaN Power High Electron Mobility Transistor (HEMT) in the DFN 5X6 package. These devices are N-channel 650 V Power GaN HEMTs based on proprietary E-mode GaN on silicon technology. The resulting product has extremely low on-state resistance, very low input capacitance and zero reverse recovery charge making it especially suitable for applications that require superior power density, ultra-high switching frequency and outstanding efficiency.



Key Features of GPI65005DF

- Ultra-low RDS(on)
- High dv/dt capability
- Extremely low input capacitance
- Zero Qrr
- Outstanding switching performance
- Low Profile

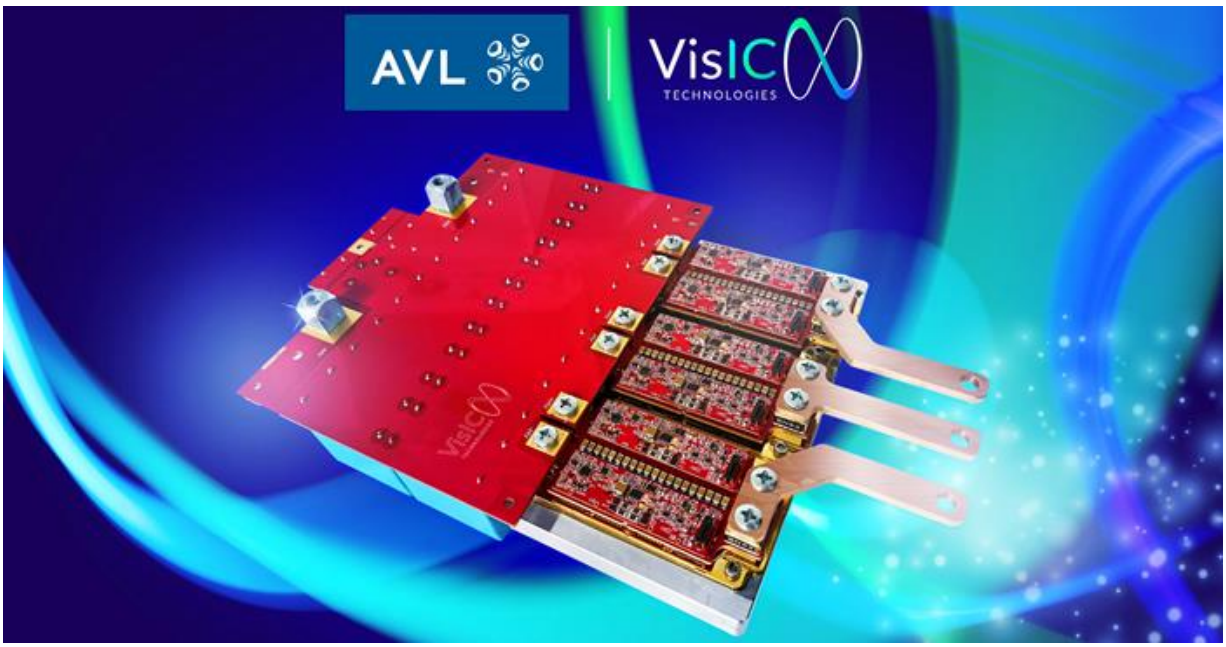
Key Applications of GPI65005DF

- Switching Power Applications
- Server and Telecom Power Application
- EVOBC and DC-DC Converters
- UPS, Inverters, Photovoltaic

VisIC and AVL Partner to Advance GaN Inverter Technology for Evs

everythingPE

VisIC Technologies, a global leader in gallium nitride (GaN) technology for electric vehicles (EVs), and AVL, a leading development partner for innovative software and hardware solutions, are proud to announce a new partnership aimed at advancing high-efficiency GaN inverter technology for the EV market. This collaboration will provide automotive OEMs with power semiconductors that exceed silicon carbide (SiC) performance, while offering lower costs at device and system level.



In a recent test conducted at AVL's state-of-the-art facilities in Germany, an inverter based on VisIC's GaN-on-Silicon D³GaN components proved an outstanding performance. Mounted on AVL's e-motor test bench and controlled by AVLs SOP eDrive controls algorithm, the system achieved a benchmark efficiency level of 99.67% at 10kHz, stunningly climbing to over 99.8% efficiency at 5kHz — which outperforms comparable SiC inverters by up to 0.5% and is cutting energy losses by more than 60%. This breakthrough positions the AVL and VisIC partnership as a compelling option for automakers striving to balance high efficiency with affordability in EV design. It is worth noting that VisIC's GaN-on-Silicon power devices require significantly less energy and therefore CO2 during the chip production process compared to SiC. They can be produced in widespread 200 mm and 300mm silicon foundries, which makes scaling production a straightforward process.

"With AVL, we're making cutting-edge GaN inverter technology accessible for even more electric vehicles, establishing a new benchmark for efficiency and cost-effectiveness in the industry," said Gregory Bunin, CTO of VisIC Technologies. "Our partnership reflects a shared commitment to driving EV innovation that's both impactful and accessible, bringing GaN's unparalleled performance to a broader market."

"Working with VisICs new GaN power module for high-power systems enables us to offer our customers cutting-edge solutions that are optimally aligned with the requirements of next-generation drive systems. These include, among other things, high power density combined with reduced overall system costs," added Dr. Thomas Frey, Head of Segment E-Mobility & E-Drive System at AVL Software and Functions GmbH. "Together, we can significantly advance e-mobility and help reduce the carbon footprint."

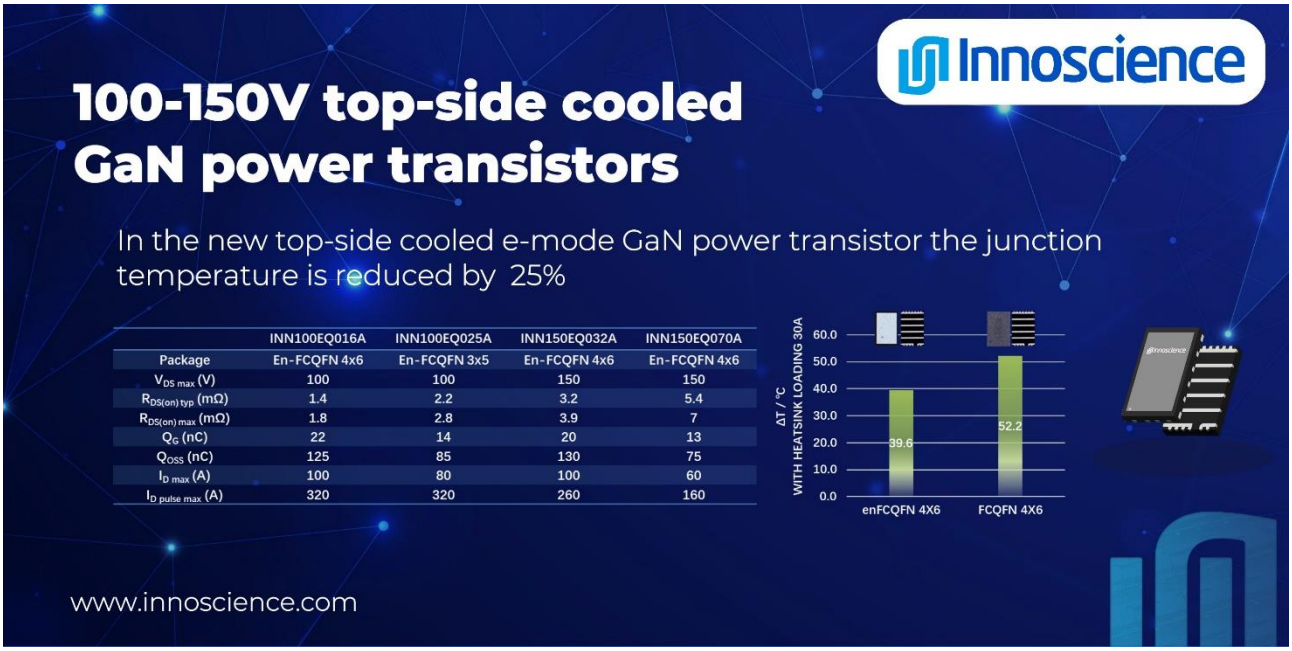
Looking ahead, AVL and VisIC plan to expand their GaN-on-Si platform to include 800V GaN power modules, ensuring that their technology remains scalable and adaptable to the needs of the growing BEV market. This collaboration places AVL and VisIC Technologies at the forefront of GaN inverter technology, establishing new standards for energy efficiency and performance across the EV industry.

Innoscience Introduces New 100-150 V Top-Side Cooled GaN Power Transistors

everythingPE

Innoscience Technology, the company founded to create a global energy ecosystem based on high-performance, low-cost, gallium-nitride-on-silicon (GaN-on-Si) power solutions, has introduced four of its GaN-on-Silicon enhancement mode high electron mobility transistors (HEMT) in its En-FCQFN top-side cooling package, resulting in significant benefits in thermal performance. For example, at 30 A, the junction temperature in the top-side cooling package is reduced from 52.2 °C for bottom-side cooling package types to 39.6 °C, a 25% improvement.

The four power GaN transistors newly released in the En-FCQFN top-side cooling package include the 100 V INN100EQ 016A/1.8mΩ and 025A/2.8mΩ parts, as well as the 150 V INN150EQ 032A/3.9mΩ and 070A/7.0mΩ devices. The pinout is compatible with bottom-side cooling package parts, and the new devices also retain the characteristics of all Innoscience parts: low resistance; low gate charge; low switching loss; extremely low reverse recovery charge; and excellent efficiency performance.



Dr. Denis Marcon, General Manager, Innoscience Europe comments: "Due to their excellent electrical properties and ultra-miniaturized packaging, our medium and low voltage GaN parts have found broad acceptance, especially in data centers, photovoltaic and energy storage systems, motor drives and power supplies for communications. The new En-FCQFN top-side cooling packaging which optimizes thermal management, further limits system temperature rise, widening the potential market."

Innoscience's 100 V~150 V GaN series are also available in WLCSP, FCQFN, LGA and other packaging types, covering different on-resistances and application areas. Together with these devices, the new top-side cooling package En-FCQFN parts are available in mass-production volumes.

Navitas Unveils GaN and SiC Innovations for AI, EVs, and Mobile Applications at CES 2025

everythingPE

Navitas Semiconductor, the only pure-play, next-generation power semiconductor company and industry leader in gallium nitride (GaN) power ICs and silicon carbide (SiC) technology, has announced that it will showcase several breakthroughs for AI data centers, EVs, and mobile technology at CES 2025 (Tech West, Venetian suite 29-335, January 7th - 10th). Navitas was recently acknowledged as the Top 500 fastest-growing technology company, by Deloitte's Technology Fast 500, for the third consecutive year.

The "Planet Navitas" suite will showcase the company's mission to 'Electrify our World' by advancing the transition from legacy silicon to next-generation, clean energy, GaN and SiC power semiconductors. These technologies are designed for high growth markets that demand the highest efficiency and power density, such as AI data centers, electric vehicles (EVs), and mobile. Additionally, Navitas will demonstrate how GaN and SiC technologies contribute to reducing carbon-footprint, with the potential to save over 6,000 megatons of CO2 per year by 2050.

Major technology and system breakthroughs include:

- World's only 650 V bi-directional GaNFast power ICs: Game-changing, disruptive GaN technology for next-generation solutions that require the highest efficiency and power density, with the lowest complexity, and significant component reduction.
- World's First 8.5 kW AI Data Center Power Supply: See the world's first 8.5 kW OCP power solution achieving 98% efficiency for AI and hyperscale data centers. Featuring high-power GaNSafe power ICs and Gen-3 Fast SiC MOSFETs in 3-Phase Interleaved CCM Totem-Pole PFC and 3-Phase LLC topologies to provide the highest efficiency, performance, and lowest component count.
- World's Highest Power Density AI Power Supply: Navitas delivers efficient 4.5 kW power in the smallest power-supply form-factor for the latest AI GPUs that demand 3x more power per rack. The optimized design uses high-power GaNSafe ICs and Gen-3 Fast SiC MOSFETs enabling the world's highest power density with 137 W/in3 and over 97% efficiency.
- 'IntelliWeave' Patented Digital Control Optimized for AI Data Center Power Supplies: Combined with high-power GaNSafe and Gen-3 'Fast' SiC MOSFETs to enable PFC peak efficiencies of 99.3% and reduce power losses by 30% compared to existing solutions.
- Automotive Qualified (AEC-Q101) Gen-3 Fast SiC MOSFETs with 'trench-assisted planar' technology: Enabled by over 20 years of SiC innovation leadership, GeneSiC technology leads on performance with the Gen-3 'Fast' SiC MOSFETs with 'trench-assisted planar' technology. This proprietary technology provides world-leading performance over temperature, delivering cool-running, fast-switching, and superior robustness to support faster charging EVs and up to 3x more powerful AI data centers.
- GaNSlim: Simple. Fast. Integrated: A new generation of highly-integrated GaN power ICs that will further simplify and speed the development of small form factor, high-power-density applications by offering the highest level of integration and thermal performance. Target applications include chargers for mobile devices and laptops, TV power supplies, and lighting systems of up to 500 W.

- SiCPAK High-Power Modules – Built for Endurance and Performance: Utilizing industry-leading 'trench-assisted planar'-gate technology and epoxy-resin potting for increased power cycling and long-lasting reliability, SiCPAK modules offer compact form factors and provide cost-effective, power-dense solutions for applications including EV charging, drives, solar, and energy storage systems (ESS).
- New Advancements in our Leading GaNFast & GeneSiC technology:
    - GaNSense motor drive ICs with bi-directional loss-less current sensing, voltage sensing, and temperature protection, further enhancing performance and robustness beyond what is achievable by any discrete GaN or discrete silicon device.
    - GeneSiC MOSFET die specifically optimized for EV traction modules with additional screening and gold metallization for sintering.
- Sustainable Solutions: Discover Navitas' vision to reduce up to 6 Gtons/year of CO2 by 2050 with technologies that offer higher efficiency, density, and grid independence.

CES 2025 takes place in Las Vegas, NV from January 7th – 10th. The "Planet Navitas" suite is located in Tech West at the Venetian, suite 29-335.

GlobalFoundries Secures $9.5 Million Funding to Advance GaN Chip Manufacturing

everythingPE

GlobalFoundries has received an additional $9.5 million in federal funding from the U.S. government to advance the manufacturing of GF's essential gallium nitride (GaN) on silicon semiconductors at its facility in Essex Junction, Vermont. The funding moves GF closer to large-scale production of GaN chips. With the ability to handle high voltages and temperatures, GaN chip technology is essential for enabling higher performance and greater energy efficiency across a range of RF and high-power control applications including automobiles, datacenter, IoT, aerospace and defense.

With the award, GF will continue to add new tools, equipment and prototyping capabilities to its market-leading GaN IP portfolio and reliability testing as the company moves closer to full-scale manufacturing of its 200mm GaN chips in Vermont. GF is committed to creating a fast and efficient path for customers to realize new innovative designs and products that leverage the unique efficiency and power management benefits of GaN chip technology.

“GF is proud of its leadership in GaN chip technology, which is positioned to make game-changing advances across multiple end-markets and enable new generations of devices with more energy-efficient RF performance and faster-charging, longer-lasting batteries,” said Nicholas Sergeant, vice president of IoT and aerospace and defense at GF. “We appreciate the U.S. government’s partnership and ongoing support of our GaN program. Realizing full-scale GaN chip manufacturing will be a catalyst for innovation, for both our commercial and government partners, and will add resilience and strengthen the semiconductor supply chain.”

The new funding, awarded by the U.S. Department of Defense’s Trusted Access Program Office (TAPO), represents the latest federal investment to support GF’s GaN program in Vermont.

“This strategic investment in critical technologies strengthens our domestic ecosystem and national security, and ensures these assets are readily available and secure for DoD utilization. In concert with key partners, this approach fortifies defense systems, empowering resilience and responsiveness,” said Dr. Nicholas Martin, Director at Defense Microelectronics Activity.

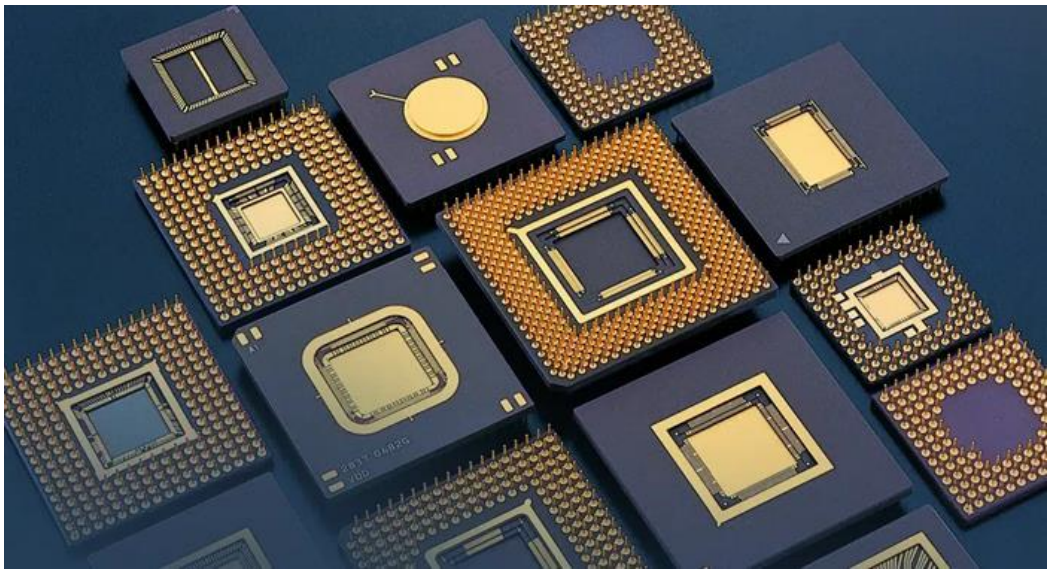
In total, including the new award, GF has received more than $80 million since 2020 from the U.S. government to support research, development and advancements to pave the way to full-scale GaN chip manufacturing.

Vermont is a U.S.-accredited Trusted Foundry and the global hub of GF’s GaN program, with longstanding leadership in 200mm semiconductor manufacturing. In July 2024, GF acquired Tagore Technology’s Gallium Nitride Power portfolio and created the GF Kolkata Power Center in Kolkata, India. The center is closely aligned with and supports GF’s facility in Vermont, and is helping advance GF’s research, development and leadership in GaN chip manufacturing.

QPT Unveils Novel Die Attach Process for Thermal Management in Power Electronics

everythingPE

The power electronics industry is facing a critical challenge. As the power handled by transistors increases to meet the needs of new applications, the packaging is increasingly struggling to remove the waste heat from the die. As a solution to this, QPT, an innovative leader in power electronics, has recently filed a patent for a novel way to attach dies to the heat spreaders or substrates which are typically Aluminum Nitride (AlN), which it calls qAttach. This provides a much better way to conduct heat away from the die and also increases reliability as the assembly process places less stress on the substrates, which is one of the biggest challenges the high-power semiconductor packaging industry faces.



QPT developed this new, qAttach process for use with the Gallium Nitride (GaN) transistors that it uses in its electric motor control designs to enable them to handle the huge amounts of waste heat that result from using them for high power, high voltage applications and at high frequency. GaN transistors are now being made that are rated for high voltages but the die size is relatively small for high-voltage transistors, which means there is less surface area to remove heat from. As a result, they are often downrated to enable them to function without overheating. qAttach solves this problem as now significantly more heat can be efficiently removed from the die so that it will not overheat. This opens up GaN to now be efficiently used for next-generation, high power, high voltage applications in automotive, and industrial motors and to finally deliver on the promise of low-cost, high voltage GaN transistors.

Rob Gwynne, QPT's CTO, said, "The problem with the current attachment approach is that the sinter layer, which fixes the die to the substrate, is typically 30 to 60 microns thick and this forms a thermal barrier that impedes the transfer of heat away from the chip. We use reliable, well-established technologies from other fields in a novel way to enable us to create the qAttach attachment layer that is potentially down to a fraction of a micron thick. This major reduction in the thermal barrier thickness means that our solution is up to ten times better at transferring waste heat away from the chip. As we refine the process, we are expecting even better thermal transmission rates through this layer."

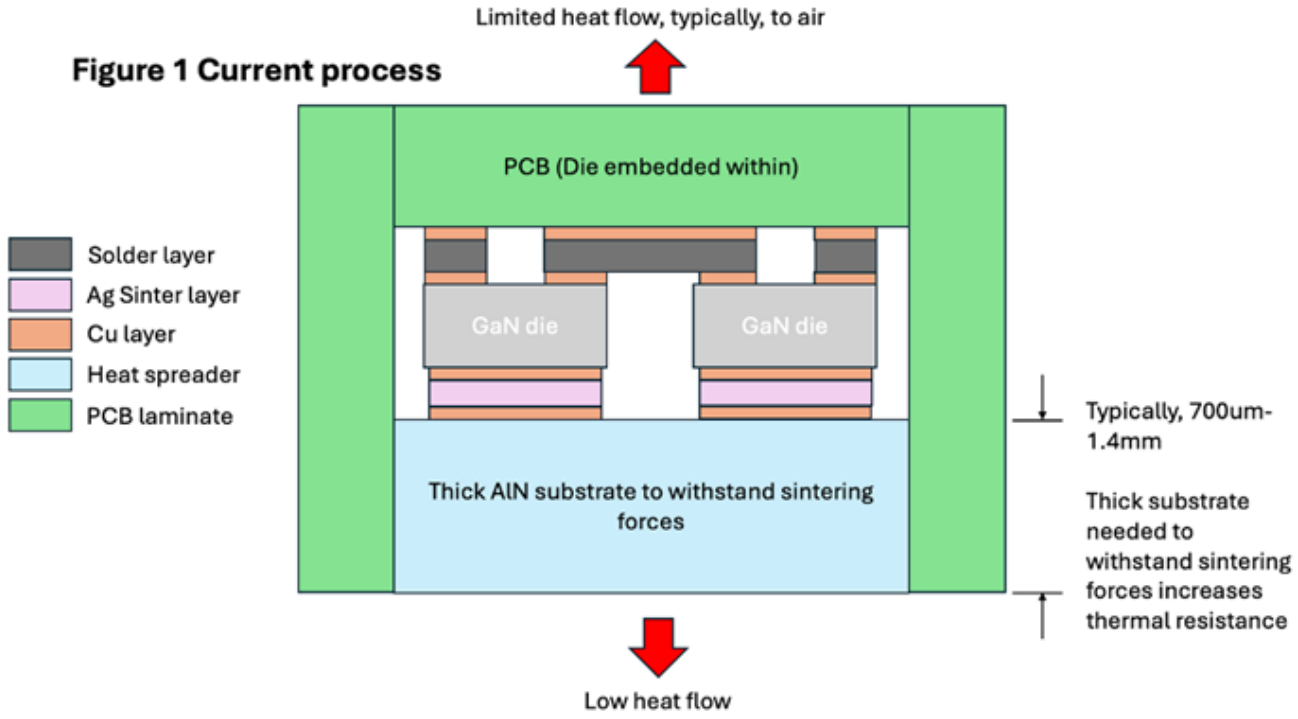


Figure 1 Current process

Gwynne explained that, with the conventional approach, the heat from the die has to pass through the thick sinter layer to the substrate to be dissipated via the heat sink as in Figure 1. The PCB is attached to the top (and around the heat spreader in embedded packages) so there is little heat dissipation that way. QPT's new structure in Figure 2 is a sandwich of heat sink, substrate, qAttach layer, die, qAttach layer, substrate and heat sink with the PCB surrounding the structure at the sides. Because the qAttach layer is ultrathin, heat can be transferred through and away much quicker plus this can also now happen from the top of the die to increase the total rate of heat removal by up to 15x.

Called qAttach, this technology has other improvements over the current sintering process. Firstly, the substrate can be much thinner as the application of the large force needed by sintering is not required. The thinner substrate significantly reduces thermal resistance to further help heat transfer away to the heat sink.

Secondly, the lower pressure required for this process means that the manufacturing stresses on the dies are less. This reduces the possibility of device failure which will be of particular interest to automotive companies where reliability is key.

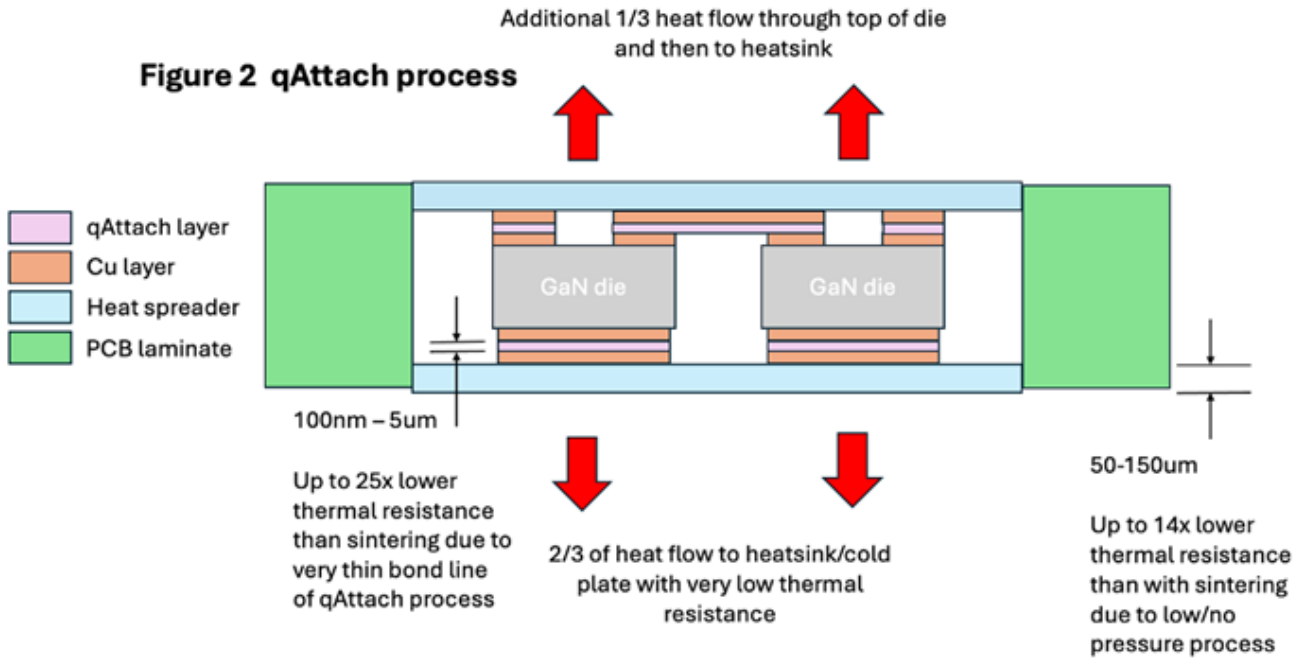


Figure 2 qAttach process

Thirdly, the ultrathin qAttach layer is not a laminar sheet. It has a proprietary geometry that constrains expansion predominantly in the Z axis, which is perpendicular to the qAttach layer when heated, so delamination of the attach layer from the die and substrate does not occur which is a major issue with current attachment methods. This is because the conventional, continuous sheet of the sintered approach has about seven times the thermal expansion of the die and about three times that of the AlN substrate. These differing rates of expansion create considerable stresses over the length of a large power die that can result in the structure ripping itself apart when heated. This delamination is the largest cause of failures in power packages so this new approach further improves the reliability of the assembled device.

Gwynne concluded, “Our new qAttach process is a universal solution to solving the growing problem of the removal of waste heat that would otherwise hold back the development of next generation, power electronics. The ability of qAttach to improve transfer heat away from the die by up to 15x can also be used to solve the removal of waste heat from almost any other type of transistors such as Silicon Carbide (SiC) to enable them to handle higher power loads than they can at present. We already have a couple of leading multinationals interested in licensing this process as they can see the strategic benefits that this innovation would bring to their product lines.”

US CHIPS Incentives Program awards finalized for BAE Systems and Rocket Lab

SemiconductorToday

BAE SYSTEMS

After completing due diligence, the US Department of Commerce has finalized two direct funding awards under the CHIPS Incentives Program's Funding Opportunity for Commercial Fabrication Facilities (following the preliminary memoranda of terms, announced on 11 December 2023 and 11 June 2024 respectively):

- up to $35.5m for BAE Systems Electronic Systems (a business unit of BAE Systems Inc, which develops and services electric propulsion technology at its facilities in Endicott, NY, USA and Rochester, UK) to support modernization of its 110,000ft2 Microelectronics Center (MEC) in Nashua, New Hampshire. This is one of few US-based defense-centric six-inch gallium arsenide (GaAs) and gallium nitride (GaN) high-electron-mobility transistor (HEMT) wafer foundries and is accredited by the Department of Defense (DoD), developing semiconductor technologies beyond those available commercially in order to meet demanding military requirements. The CHIPS funding will enable the firm to quadruple its production capacity for monolithic microwave integrated circuit (MMIC) chips (which are critical components for advanced military aircraft and commercial satellite systems) and replace aging tools with the latest technology and equipment (mitigating the risk of an operational disruption). The investment will also cut the firm's modernization timeline in half, bolstering the facility's ability to serve mission-critical defense programs.
- up to $23.9m for Rocket Lab (the parent company of space power provider SolAero Technologies Corp) to create a more robust and resilient supply of space-grade solar cells that power spacecraft and satellites. Rocket Lab is one of two companies in the USA that specialize in the production of highly efficient and radiation-resistant compound semiconductor space-grade solar cells. Rocket Lab's are key to US space programs such as missile awareness systems and science missions, including the James Webb Space Telescope, NASA's Artemis program, the Ingenuity Mars Helicopter, and the Mars Insight Lander. Rocket Lab's technology also serves a growing commercial satellite market. The funding will support the modernization and expansion of Rocket Lab's facility in Albuquerque, NM, which will increase the company's compound semiconductor production by 50% within the next three years – helping to meet the growing national security and commercial demand for these solar cells in the USA. The investment is expected to create over 100 direct jobs.

"From satellites in space to defense systems on the ground, our most advanced defense and commercial technology rely on mature-node and compound semiconductors to operate," says Under Secretary of Commerce for Standards and Technology and National Institute of Standards and Technology director Laurie E. Locascio. "By finalizing these awards, we are strengthening America's domestic semiconductor supply chain resilience and broadening our manufacturing capabilities."

"America's space and military systems are the most capable in the world, and that would not be possible without advanced semiconductor technology," says Arati Prabhakar, assistant to the President for Science and Technology and director of the White House Office of Science and Technology Policy. "We're making the semiconductor supply chain investments today that will bolster American global competitiveness and security tomorrow," she adds.

"This investment marks a significant step forward for the modernization of our Microelectronics Center, enhancing our national security," comments Cheryl Paradis, VP & general manager of FAST Labs at BAE Systems Inc. "We

remain committed to driving innovation, developing a highly skilled workforce, and ensuring that the US maintains its edge in the critical aerospace and defense industry," she adds.

"This award will help to ensure US leadership in compound semiconductor manufacturing capability while reinforcing Rocket Lab's position as a leader in space-grade solar cell production," says Brad Clevenger, VP of Rocket Lab Space Systems. "The investment will enable Rocket Lab to expand production, create highly skilled manufacturing jobs and generate economic and workforce development activity in New Mexico."

As stated in the CHIPS Notice of Funding Opportunity for Commercial Fabrication Facilities, CHIPS for America is disbursing direct funding to recipients for capital expenditures based on the completion of project construction, production and commercial milestones. The program will track the performance of each CHIPS Incentives Award via financial and programmatic reports, in accordance with the award terms and conditions.

Penn State gains $3m DARPA grant for GaN-on-silicon project with Northrop Grumman

SemiconductorToday

Penn State is to receive $3m from the US Defense Advanced Research Projects Agency (DARPA) as part of a larger grant awarded to defense, aerospace and technology company Northrop Grumman. The joint project aims to develop a novel method for integrating gallium nitride (GaN) with silicon substrates, since GaN provides superior performance and faster switching speeds for power-intensive applications while silicon offers scalability and affordability. This hybrid approach can lead to more efficient power electronics with lower production costs, suiting high-demand applications like electric vehicles, power electronics and data centers, where efficiency and durability are critical.

"Silicon is the common platform for microelectronics but it is challenging to combine new semiconductor materials with silicon," says Joan Redwing, distinguished professor of materials science and engineering and director of the Penn State Materials Research Institute's (MRI) Two-Dimensional Crystal Consortium, a US National Science Foundation Materials Innovation Platform and national user facility. "To overcome this, we need new approaches to densely integrate advanced materials with silicon," she adds. "Our work with Northrup Grumman is designed to explore integrating gallium nitride directly onto silicon using two-dimensional materials as interlayers."

To achieve this, with the DARPA grant Penn State will work with Northrup Grumman to develop heterogeneous integration using 2D materials that are one to a few atoms thick, such as molybdenum disulfide and gallium selenide, as seed layers to grow GaN on industry-compatible silicon (001), which is the preferred crystal orientation used in existing semiconductor manufacturing. A seed layer provides a template or foundation that influences the structure, orientation and quality of the material grown on top.

"The current approach to gallium nitride-on-silicon integration has too many drawbacks, from increased thermal resistance to device fabrication challenges on silicon (001)," says Joshua Robinson, professor of materials science and engineering and Penn State's principal investigator on the DARPA project. "By using 2D materials as seed layers, we aim to eliminate these issues and develop a direct route to integrating gallium nitride-on-silicon with improved performance compared to current technologies. This could directly impact manufacturing costs and enable market entry into energy-efficient devices."

The project will leverage Penn State's infrastructure for growing and characterizing 2D materials and wide-bandgap semiconductors. "This program allows us to demonstrate that 2D materials could be key to enabling advances in 3D semiconductors," Robinson says. "We're combining our expertise in 2D research with the real-world need for improved semiconductor performance, setting the stage for years of innovation in heterogeneous integration."

The equipment and methodologies developed through this grant will be available to other researchers through MRI's user facilities, Robinson says, with the goal of fostering collaboration and innovation among a variety of partners.

EPC launches GaN FET-based reference design for solar PV optimizers

SemiconductorToday

Efficient Power Conversion Corp (EPC) of El Segundo, CA, USA — which makes enhancement-mode gallium nitride on silicon (eGaN) power field-effect transistors (FETs) and integrated circuits for power management applications — has launched the EPC9178, the latest reference design for photovoltaic (PV) optimizers. Designed to deliver high reliability while addressing critical challenges in energy efficiency and cost-effectiveness through the reduction of passive components in solar energy systems, the EPC9178 demonstrates the transformative potential of GaN technology for renewable energy solutions, says the firm.

The EPC9178 reference design employs a back-to-back buck-boost converter topology, ensuring optimal energy harvesting for each solar panel, even under challenging conditions such as shading. The compact, high-performance solution bridges the gap between micro-inverters and string inverters, offering enhanced energy efficiency and compatibility with existing infrastructure.

The EPC9178 combines GaN technology with a dedicated controller to deliver what is claimed to be unmatched performance and reliability. Features include:

- Compact design: High-frequency operation at 450kHz minimizes the size of passive components, resulting in a lightweight and space-saving solution.

- High efficiency: up to 98% peak efficiency, reducing power losses and improving thermal management.
- Advanced GaN technology: Powered by 100V-rated EPC2306 eGaN FETs, the EPC9178 offers low on-resistance (3.8mΩ) and reduced switching losses compared with silicon MOSFETs.
- Simplified control: An integrated LM5177 controller from Texas Instruments reduces design complexity and component count.
- Versatile output settings: Operates across an input voltage range of 30–60V, with selectable output voltages of 30V, 45V and 60V.

"The EPC9178 delivers a compact, high-performance and reliable design that enables cost-effective solar energy systems," says CEO Alex Lidow.

The EPC9178 evaluation boards are priced at $480. The EPC2306 is priced at $1.87 each in 3Ku reels. Evaluation boards and devices are available for immediate delivery from distributor Digi-Key Corp.

ST launches 250W MasterGaN reference design, fast-tracking compact, efficient industrial power supplies

SemiconductorToday

STMicroelectronics of Geneva, Switzerland has launched the EVL250WMG1L resonant-converter reference design based on its MasterGaN1L system-in-package (SiP), as the firm continues to accelerate the design of gallium nitride (GaN) power supplies (PSUs) that deliver superior efficiency and power density.

ST's MasterGaN SiPs combine GaN power transistors with gate drivers specially optimized to ensure fast and controlled switching. Using these SiPs in place of an equivalent network of discrete components helps to maximize performance and reliability while also accelerating design and saving PCB space, ST says.

The new reference design targets industrial applications where space is limited and efficiency is critical. Combining the MasterGaN1L, which contains two 650V 150mΩ GaN FETs, with ST's L6599A resonant controller, the PSU achieves peak efficiency of over 94% and operates without heat-sinks on the primary side. Also leveraging ST's SRK2001A synchronous-rectification controller, the unit has a compact overall footprint of 80mm x 50mm and power density of 34W/inch3.

The PSU can deliver up to 10A output current (equivalent to 250W at 24Vdc) while also having standby current consumption below 1µA, aiding energy saving. Protection features built into the L6599A and SRK2001A ensure resilience against overcurrent, short-circuit and over-voltage, while input-voltage monitoring ensures correct startup and provides under-voltage lockout.

The EVL250WMG1L is available now, fully built and ready for evaluation, for $250.

Navitas ranked in Deloitte Technology Fast 500 list for third consecutive year

SemiconductorToday

Navitas

Navitas Semiconductor Corp of Torrance, CA, USA says that its revenue growth has been acknowledged for the third consecutive year by being ranked in Deloitte's Technology Fast 500 list. Navitas' growth was driven by strong demand for its high-efficiency, wide-bandgap gallium nitride (GaN) and silicon carbide (SiC) power components across a growing number of global markets and customers.

Now in its 30th year, the Fast 500 ranks the fastest-growing technology, media, telecoms, life sciences, fintech, and energy tech companies — both public and private — in North America. Based on percentage fiscal year revenue growth from 2020 to 2023, Navitas achieved 571% growth as GaN and SiC technology enabled efficient, sustainable applications and displaced legacy silicon chips, says the firm.

"As a 'pure-play' next-gen semiconductor company, Navitas continues to outperform the overall power semiconductor market, with record sales into mobile fast chargers, now ramping AI data-center revenues and a strong customer pipeline for EV opportunities," says CEO & co-founder Gene Sheridan. "Recent introductions like GaNSafe, Gen-3 'Fast' SiC, and a newly announced 48V-focused range in partnership with Infineon, have built a strong foundation for further revenue growth in applications from 20W to 20MW, and with a market opportunity of over $22bn per year."

Sener coordinates SAGaN, the international consortium that will develop next-generation space electronics

Sener

sener

The Sener engineering and technology industrial group participates in the international SAGaN consortium, an acronym in English for gallium nitride transistor for space applications, whose objective is the development of next-generation electronic components for especially demanding space missions and applications.

Sener is the company responsible for coordinating this consortium, in which Semi Zabala, Imec and Disco Hi-Tec Europe GmbH collaborate as partners, and will also be in charge of manufacturing original equipment for spacecraft and instruments that use gallium nitride transistors.

SAGaN aims to develop high-voltage gallium nitride transistors, an essential innovation for creating more advanced and efficient electronic equipment for space missions. These transistors offer higher performance than traditional silicon-based components. Gallium nitride transistors will therefore enable lighter and more efficient spacecraft that can withstand the extreme conditions of space, including radiation and vacuum-like pressures.

The consortium partners have the experience needed to carry out all operations for creating 650 V gallium nitride transistors for space, from design and manufacturing to processing and testing. This ability to create a complete supply chain for this type of transistors will strengthen the continent's competitiveness in the aerospace industry.

"SAGaN not only reinforces our commitment to innovation and excellence in the aerospace industry, but also has the potential to raise energy efficiency standards in space, reducing the load on power systems and increasing the lifetime of missions," highlights Miguel Pérez, Power Electronics Coordinator at Sener.

CGD Demos 800 VDC Multi-Level Inverter Developed Using GaN With IFPEN That Outperforms SiC

Cambridge GaN Devices

Cambridge, UK - Cambridge GaN Devices (CGD), the fabless, clean-tech semiconductor company that develops energy-efficient GaN-based power devices that make greener electronics possible, and IFP Energies nouvelles (IFPEN), a major French public research and training organization in the fields of energy, transport and the environment, have developed a demo which confirms the suitability of CGD's ICeGaN®650 V GaN ICs in a multi-level, 800 VDC inverter. The demo delivers super-high power density – 30 kW/l - which is greater than can be achieved by more expensive, state-of-the-art silicon-carbide (SiC)-based devices. The inverter realization also demonstrates the ease of paralleling that ICeGaN technology enables; each inverter node has three 25mΩ / 650V ICeGaN ICs - 36 devices in total - in parallel.

ANDREA BRICCONI | CHIEF MARKETING OFFICER, CGD

"We are super excited at this first result of our partnership with IFPEN. 800 VDC supports the 800 V bus which is being increasingly adopted by the EV industry. By addressing automotive and other high voltage inverter applications with energy-efficient ICeGaN-based solutions we are delivering on CGD's key commitment – sustainability."

This multi-level GaN Inverters can power electric motors to over 100 kW peak, 75 kW continuous power. The CGD/IFPEN demo features: a high voltage input of up to 800Vdc; 3-phase output; a peak current of 125 Arms (10s) (180 Apk); and a continuous current of 85 Arms continuous (120 Apk).

The ICeGaN multi-level design proposed by IFPEN reveals several compelling benefits:

- **Increased Efficiency**: the improvement in the efficiency of the traction inverter leads to an increase in battery range and a reduction in charging cycles. It also leads to a reduction in battery cost if the initial range (iso-range) is maintained;

- **Higher switching frequencies**: GaN transistors can operate at much higher frequencies than silicon transistors. This reduces iron losses in the motor, particularly in the case of machines with low inductances;
- **Reduced Electromagnetic Interferences**: 3-level topology minimizes EMI and enhances the reliability of the system;
- **Enhanced thermal management**: insulated metallized substrate boards featuring an aluminium core facilitate superior thermal dissipation, ensuring optimal operating temperatures and extending the lifespan of the system and associated GaN devices;
- **Modular design**: this facilitates scalability and adaptability for varying system requirements.

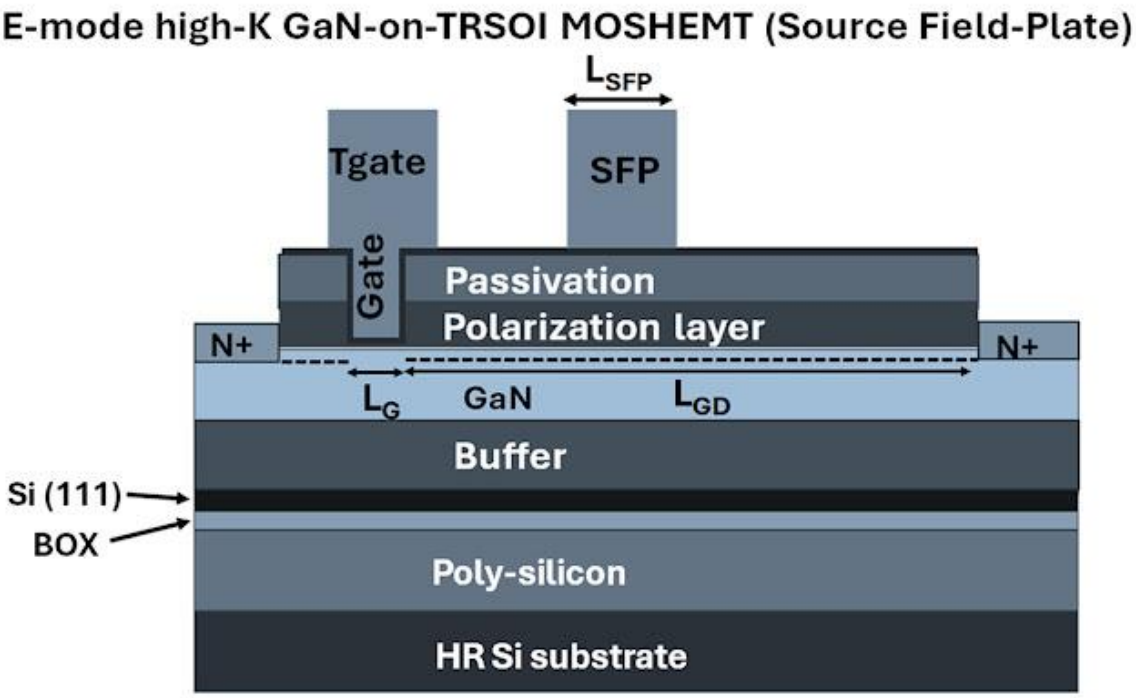
GAETANO DE PAOLA | PROGRAM MANAGER, IFPEN

"Following the implementation of this inverter reference using CGD's enabling ICeGaN ICs coupled with innovative topologies, such as multi-level solutions, IFPEN now strongly believes that GaN is a breakthrough technology in terms of performance and cost for high-voltage traction inverters."

Intel Pushes Gallium Nitride (GaN) Technology to New Heights with 300mm GaN-on-TRSOI Substrates

BALD Engineering

Intel Foundry continues to redefine the future of semiconductor technology with groundbreaking advancements in gallium nitride (GaN) technology. At the IEEE International Electron Devices Meeting (IEDM) 2024, Intel showcased the industry's first 300mm GaN-on-TRSOI substrates, setting a new benchmark for high-performance power and radio frequency (RF) electronics. This innovation is part of Intel's larger commitment to solving critical challenges in AI, energy efficiency, and thermal management.



The use of 300mm GaN-on-TRSOI substrates enables superior performance by reducing signal loss and enhancing signal linearity. These substrates are engineered to support advanced integration schemes through backside substrate processing, offering significant benefits for applications in RF and power electronics. One of the standout achievements demonstrated was the fabrication of 30nm channel-length enhancement-mode GaN MOSHEMTs (metal-oxide-semiconductor high electron mobility transistors). These transistors achieved remarkable performance metrics, including an Ron x Coff of 80 femtoseconds and an fmax exceeding 500 GHz, making them ideal for cutting-edge RF switches.

Intel's advancements in GaN technology are complemented by its focus on advanced memory integration, hybrid bonding, and modular system expansion. These innovations are designed to address the growing demands of AI and other high-performance computing applications, paving the way for more energy-efficient and thermally optimized systems. By pushing the boundaries of materials and integration technologies, Intel is positioning itself as a leader in driving semiconductor advancements for the trillion-transistor era.

OTHER

AIXTRON to Advance in Compound Semiconductor Technology

everythingPE

AIXTRON

AIXTRON, a leading provider of deposition equipment to the semiconductor industry, has opened its new Innovation Centre at the company's headquarters in Herzogenrath. Mona Neubaur, Minister for Economic Affairs of the State of North Rhine-Westphalia, opened the Innovation Centre. At the official ceremony, AIXTRON CEO Dr. Felix Grawert and CFO Dr. Christian Danninger showed the minister the new research and development complex with 1,000 m² of cleanroom space. It lays the foundation for the transition to 300 mm wafer size in the Compound Semiconductor Industry.

“AIXTRON's new innovation center is an impressive example of the innovative strength and future viability of the semiconductor industry in North Rhine-Westphalia. The launch of 300 mm wafer technology is a milestone for the energy efficiency and competitiveness of our region. Our global competitiveness benefits enormously from robust domestic semiconductor production because semiconductors are essential for the transformation towards climate neutrality: without them, no computer would run, no car would drive, and neither wind nor solar plants could produce energy,” said Mona Neubaur, Minister for Economic Affairs, Industry, Climate Protection and Energy and Deputy Prime Minister of the State of North Rhine-Westphalia.

The event was attended by representatives from the world of politics, the city of Herzogenrath, the Aachen Chamber of Industry and Commerce, and the media. The minister visited AIXTRON as part of an innovation tour in North Rhine-Westphalia.

“With the new 300mm-capable cleanroom at the Innovation Center, we will further expand our technological market leadership,” said Dr. Felix Grawert, President and CEO of AIXTRON SE. ”We already have the first 300 mm GaN prototype systems, which have also been integrated into pilot lines at several customers. And this is precisely where AIXTRON's innovative strength and DNA come into play. For decades, we have been working on technological solutions even when the market had not yet defined its requirements in concrete terms. This enables us to help our customers with their product developments at an early stage and to offer innovative technologies that are market-ready at precisely the moment when demand first arises.”

The groundbreaking ceremony and start of construction of the state-of-the-art complex, in which AIXTRON is investing around 100 million euros, was in November 2023. The high-tech building is designed for the next big step in compound semiconductor technology: the important transition to 300 mm wafer size for gallium nitride (GaN) and other Compound Semiconductor applications. The GaN material system, in which AIXTRON is the technology leader, is being used in an increasing number of power electronics applications due to its outstanding material properties. GaN-based semiconductor devices increase the efficiency of chargers in consumer electronics, enable efficient power conversion in the field of renewable energy, and provide energy-efficient power supply for servers and data centers. This also helps, for example, with the applications for artificial intelligence, which are currently spreading rapidly, because these require a great deal of energy.

To prepare for this demand, AIXTRON is driving forward the development of 300 mm deposition technology. The larger wafer size offers customers the productivity gain of 2.25 times more wafer area compared to the currently used 200 mm wafers. Furthermore, customers can use their 300 mm fabs and processing equipment for the first time in the field of Compound Semiconductors. This will make the production of GaN semiconductor devices not only more cost-effective but also offer opportunities for technology performance gains in the future.

“With 300mm wafer technology, we are bringing Compound Semiconductors for the first time into the mainstream of semiconductor fabrication. The Innovation Center is a major element of our strategy, providing space and capabilities for next-generation technologies. The step towards 300 mm in Compound Semiconductors is a landmark milestone, that is set to trigger numerous growth options for the industry in the years to come.” explains Professor Dr. Michael Heuken, Vice President of Advanced Technologies at AIXTRON.

Vishay investing £51m in Newport Wafer Fab

SemiconductorToday

Discrete semiconductor and passive electronic component maker Vishay Intertechnology Inc of Malvern, PA, USA is investing £51m in Newport Wafer Fab in South Wales (the UK's largest semiconductor wafer fabrication facility, which it acquired from Nexperia in March for $177m, or about £142m), bringing new product range capabilities and skilled job opportunities to what is now Newport Vishay.

The investment has been supported by £5m in funding from the Welsh Government, which cites other recent progress in the South Wales compound semiconductor cluster including:

- US-owned KLA is constructing its new European headquarters at Imperial Park, Newport. With Welsh Government investment in the grid infrastructure at the site, the 215,000ft2, $100m development is creating an innovation centre and manufacturing facility and will include cleanrooms for R&D and manufacturing. Recruitment of up to 750 staff is already underway.
- Centre 7, a facility supported by Welsh Government as part of its International Strategy, is already attracting inward investors, with Microlink Devices and CS Connected the first tenants at the 51,000ft2 Cardiff Gate site.
- a £2.5m Net Zero research project at Swansea University's Centre for Semiconductor Materials is pioneering the reduction of building emissions for the semiconductor industry and has research agreements with industrial members such as Vishay, which counts a number of Swansea alumni amongst its executives.
- Cardiff University hosted an international technical conference in October on semiconductor power devices, and Wales will welcome an inward mission by Canadian semiconductor companies next Spring.

"Compound semiconductors are all around us – in our homes and in our phones, our trains and our turbines. They are a vital, if miniature, piece of what makes the modern world tick, with extremely strong global growth projections. And we in Wales are increasingly a world-leading nation in their production and manufacture," states Rebecca Evans, the Welsh Government's Economy, Energy and Planning Cabinet Secretary. "Today that is more evident than ever, with our international reputation attracting significant inward investment, the provision and occupation of state-of-the-art facilities, clear links with R&D, and well-paid opportunities for employment and apprenticeships," she adds. "We are now, after a decade of seeding the cluster, reaping the rewards of our commitment, which we will continue to drive forward."

China bans export of critical minerals to US as trade tensions escalate

Reuters

- Beijing's curbs follow latest US limits on Chinese chip sector
- Exports of gallium, germanium to US already stalled
- Antimony prices surge this year as China stifles exports

Dec 3 (Reuters) - China on Tuesday banned exports to the United States of the critical minerals gallium, germanium and antimony that have widespread military applications, escalating trade tensions the day after Washington's latest crackdown on China's chip sector.

The curbs strengthen enforcement of existing limits on critical minerals exports that Beijing began rolling out last year, but apply only to the U.S. market, in the latest escalation of trade tensions between the world's two largest economies ahead of President-elect Donald Trump taking office next month.

A Chinese Commerce Ministry directive on dual-use items with both military and civilian applications cited national security concerns. The order, which takes immediate effect, also requires stricter review of end-usage for graphite items shipped to the U.S.

"In principle, the export of gallium, germanium, antimony, and superhard materials to the United States shall not be permitted," the ministry said.

Gallium and germanium are used in semiconductors, while germanium is also used in infrared technology, fibre optic cables and solar cells. Antimony is used in bullets and other weaponry, while graphite is the largest component by volume of electric vehicle batteries.

The move has sparked fresh concern that Beijing could next target other critical minerals, including those with even broader usage such as nickel or cobalt.

"China has been signalling for some time that it's willing to take these steps, so when is the U.S. going to learn its lesson?" said Todd Malan of Talon Metals (TLO.TO), opens new tab, which is trying to develop a nickel mine in Minnesota and is exploring for the metal in Michigan. The only U.S. nickel mine will be depleted by 2028.

The United States was assessing the new restrictions, but will take "necessary steps" in response, a White House spokesperson said, without giving details.

"These new controls only underscore the importance of strengthening our efforts with other countries to de-risk and diversify critical supply chains away from PRC (China)," the spokesperson said.

Representatives for Trump did not immediately respond to a request for comment.

Chinese customs data show there have been no shipments of wrought and unwrought germanium or gallium to the U.S. this year through October, although it was the fourth and fifth-largest market for the minerals, respectively, a year earlier.

Similarly, China's overall October shipments of antimony products plunged by 97% from September after Beijing's move to limit its exports took effect.

China accounted last year for 48% of globally mined antimony, which is used in ammunition, infrared missiles, nuclear weapons and night-vision goggles, as well as in batteries and photovoltaic equipment.

This year, China has accounted for 59.2% of refined germanium output and 98.8% of refined gallium production, according to consultancy Project Blue.

"The move is a considerable escalation of tensions in supply chains where access to raw material units is already tight in the West," said Project Blue co-founder Jack Bedder.

Prices of antimony trioxide in Rotterdam had soared by 228% since the beginning of the year to $39,000 a metric ton on Nov. 28, data from information provider Argus showed.

"Everyone will dig in their backyard to find antimony. Many countries will try to find antimony deposits," said a minor metals trader in Europe, declining to be named.

Perpetua Resources (PPTA.O), opens new tab, which is developing an Idaho antimony mine with U.S. government financial support, said China is "weaponizing accessing" to minerals critical for the U.S. military and technology firms.

"We must get serious about American mineral sources," said Perpetua CEO Jon Cherry. "It's time to end our reliance on China and secure our future."

United States Antimony (UAMY.A), opens new tab, which refines antimony in Montana, said it believes China's move will boost prices of the metal and thus increase supplies for its smelter, although the company acknowledged that it will take time for mines to be developed.

China's announcement comes after Washington launched its third crackdown in three years on China's semiconductor industry on Monday, curbing exports to 140 companies, including chip equipment maker Naura Technology Group (002371.SZ), opens new tab.

Trump, whose first four-year White House term was marked by a bitter trade war with China, has said he will implement 10% tariffs on Chinese goods and threatened 60% tariffs on Chinese imports during his presidential campaign.

"It comes as no surprise that China has responded to the increasing restrictions by American authorities, current and imminent, with its own restrictions on the supply of these strategic minerals," said Peter Arkell, chairman of the Global Mining Association of China.

"It's a trade war that has no winners," he said.

Separately, several Chinese industry groups on Tuesday called for their members to buy domestically made semiconductors, with one saying U.S. chips were no longer safe and reliable.

Nexperia to comply with U.S. restrictions on Chinese parent Wingtech

Reuters

AMSTERDAM, Dec 3 (Reuters) - Nexperia, a Dutch-based computer chip maker, will comply with U.S. restrictions after its Chinese parent company Wingtech (600745.SS), opens new tab was put on the U.S. Department of Commerce's "entity list", a spokesperson said on Tuesday.

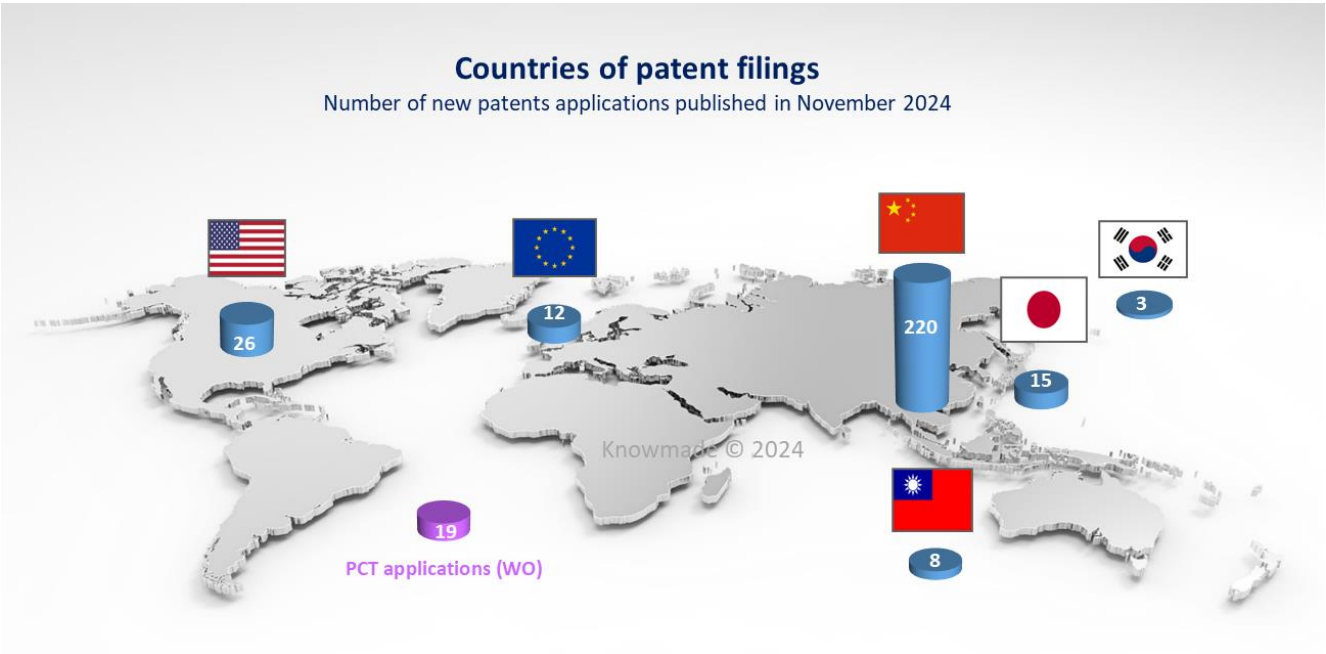
"The listing subjects Wingtech’s access to U.S. technology to licensing requirements," the spokesperson said. "These do not apply to Nexperia or its subsidiaries. Nexperia will comply with the U.S. restrictions as these apply to its interactions with Wingtech."

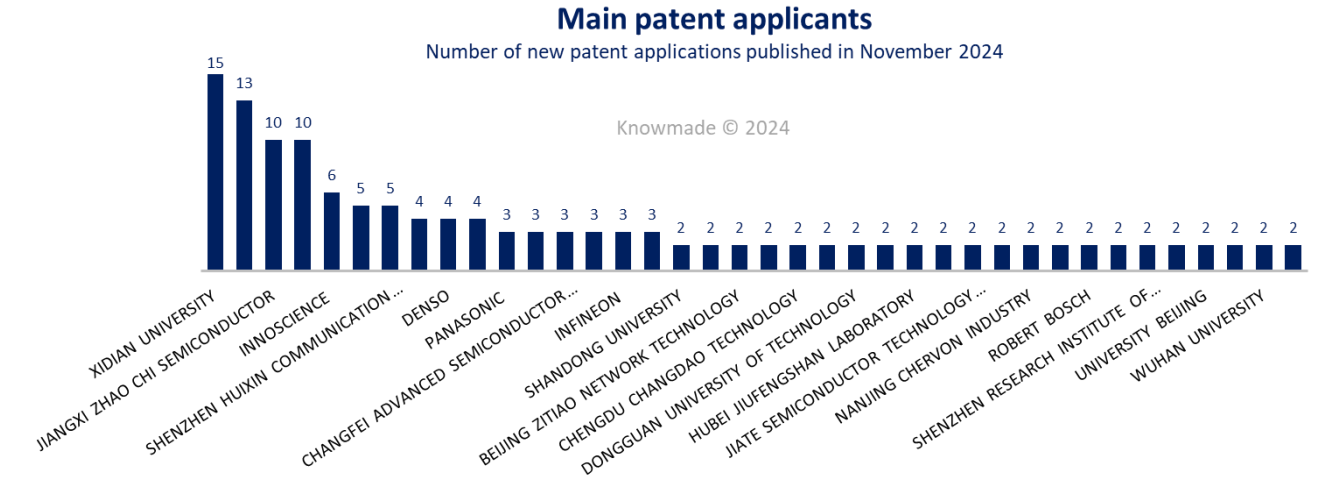
Nexperia is one of the world's largest makers of simple computer chips such as diodes and transistors, and this year it moved to expand operations in Hamburg, Germany.

The Commerce Department said on Monday it had added Wingtech and several Chinese investment firms to the list due to their efforts to acquire chip manufacturing technology critical to the defence industry of the U.S. and its allies.

PATENT APPLICATIONS

More than 260 **new patent families (inventions)** were published last month.





Other patent applicants: Xi An Zhong Che Yongdian Electric, Yangzhou Guoyu Electronics, ADE Technologies, Allegro Microsystems, Anhui East China Photoelectric Technology Research Institute, Applied Materials, Asahi Kasei, Audisankara College of Engineering Technology, Beijing Chenjing Electronic, Beijing Naura Microelectronics Equipment, Beijing Zhongdianke Satellite Navigation System, Brown University, Cambridge GaN Devices, Chiba University, China Resources Microelectronics Chongqing, China Zhenhua Yongguang Electronics, Chongqing Kangjia Optoelectronic Technology, Delta Electronics, Dongguan Institute of Opto Electronics Peking University, Dugen Hexin Photoelectric Technology Suzhou, Dugen Photoelectric Technology Nantong, East China Institute of Technology, East China Normal University, Electric Power Research Institute of China, Embex, Foshan Lighting Zhida Electrician Technology, Foshan Power Supply Bureau Guangdong Power Grid, Fuji Electric, Ganext Zhuhai Technology, GlobalFoundries, Guangdong Power Grid, Guangfei Digital Technology Guangzhou, Guangzhou Chinaray Optoelectronic Materials, Hangzhou Dianzi University, Hangzhou Huawei Ouyuan Technology, Hangzhou Xiantuo Electronic Technology, Hangzhou Yunjia Semiconductor Technology, Hefei IC Valley Microelectronics, Heyuan Choicore Photoelectric Technology, Huawei, Hubei University, Hunan Lanxin Microelectronic Technology, Hunan Normal University, Hyper Electronics, Indian Institute of Technology Roorkee, Intel, IVWorks, Japan Display, Jiangsu Institute of Advanced Semiconductors, Jiangsu Ocean University, Jiangsu University, Jiangsu Zunyang Electronic Technology, Jiangxi Advanced Research Institute, Jiangxi Ronghong Brocade Material Science & Technology, Jiangxi Science & Technology Normal University, L D Electronics, Latticepower, Lextar Electronics, Maxscend Microelectronics, Mirise Technologies, MIT - Massachusetts Institute of Technology.

OPTOELECTRONICS

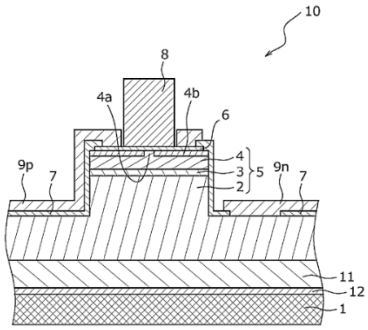
Notable new patent applications selected by Knowmade

GaN VCSEL having an improved reflectance of a multilayer reflective film

Publication Number: US20240396303

Patent Applicant: Nichia

A vertical cavity surface emitting laser element includes a substrate, an AlGaN foundation layer, a multilayer reflective film, and an n-side semiconductor layer, an active layer, and a p-side semiconductor layer. The substrate contains GaN. The AlGaN foundation layer is arranged on an upper surface of the substrate. The multilayer reflective film is arranged on an upper surface of the foundation layer and including an AlInN layer. The n-side semiconductor layer, the active layer, and the p-side semiconductor layer are arranged above the multilayer reflective film.

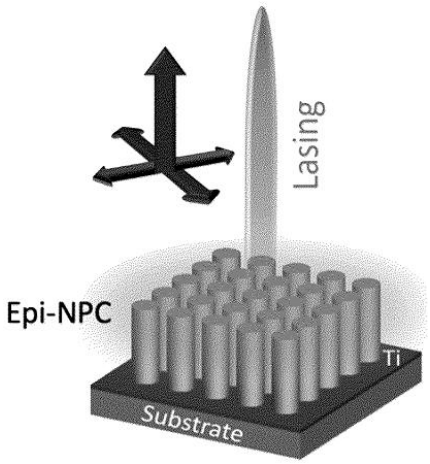


Method of manufacturing a more uniform array of GaN nanowires using MBE and SAG

Publication Number: US20240396300

Patent Applicant: MCGILL University

There is described a method of manufacturing an array of GaN nanowires via selective area growth. The method generally has: mounting a substrate to a substrate holder face exposed within a growth cavity, the substrate having a base layer and a mask covering the base layer, the mask having a plurality of apertures spaced apart from one another and exposing the base layer thereunder; while heating the growth cavity at a given surface temperature ranging between about 650° C. and 750° C. when measured on a side of the substrate holder face to which the substrate is mounted, directing gallium (Ga) and nitrogen (N) atoms towards the selective area growth mask at a gallium growth rate below about 10 nm/min and a nitrogen growth rate below 5 nm/min, respectively, said heating and said directing selectively growing the GaN nanowires at corresponding ones of the apertures.

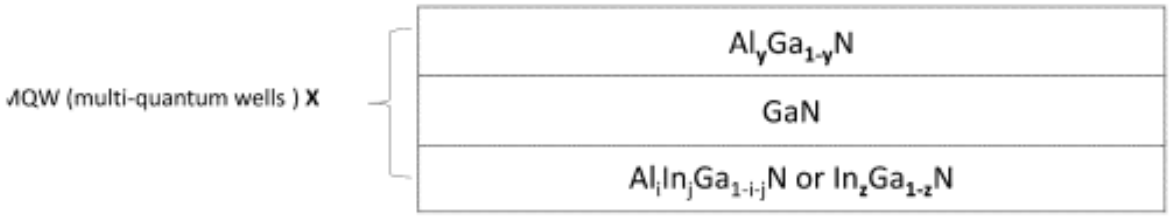


Light-emitters with group III-nitride-based quantum well active regions having GaN interlayers

Publication Number: US20240395966

Patent Applicant: University of Wisconsin

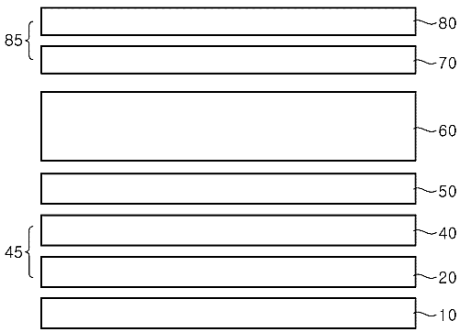
Group III-nitride-based light-emitting devices are provided. The light-emitting devices are characterized by an active region having one or more quantum wells. The one or more quantum wells having a double well design provided by a first well layer comprising an AlInGaN alloy or an InGaN alloy and an adjacent GaN interlayer, both of which are disposed between two barrier layers comprising an AlGaN alloy or a low-In-content AlInGaN alloy.



LED emitting light of multi peak wavelengths

Publication Number: US20240379905

Patent Applicant: Seoul Viosys



An LED according to an exemplary embodiment of the present disclosure includes a 1st conductivity type semiconductor layer; an active region including a barrier layer and a well layer; a strain control layer disposed between the 1st conductivity type semiconductor layer and the active region; a superlattice layer disposed between the strain control layer and the active region; a 2nd conductivity type semiconductor layer disposed on the active region; and an electron blocking layer disposed between the active region and the 2nd conductivity type semiconductor layer, in which the 1st conductivity type semiconductor layer and the well layer are represented by a predetermined formula, and a ratio of a mole fraction of In to a mole fraction of Ga in the 1st conductivity type semiconductor layer and a ratio of a mole fraction of In to a mole fraction of Ga in the well layer satisfy a predetermined equation.

GaN-based laser with enhanced modulation bandwidth

Publication Number: WO2024/244973

Patent Applicant: Huawei and Institute of Semiconductors (CAS)

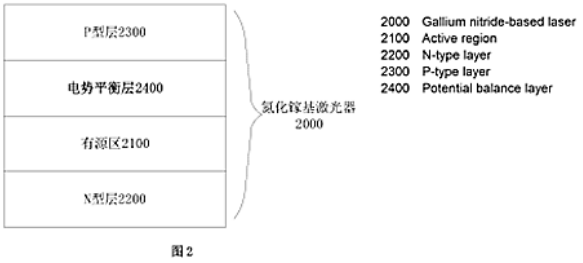


图2

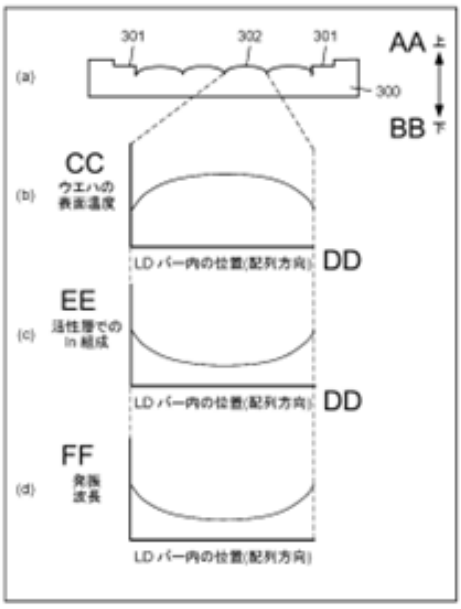
A GaN-based laser (2000), comprising an active region (2100), an N-type layer (2200) and a P-type layer (2300), wherein the N-type layer (2200) is used for providing electrons to the active region (2100); the P-type layer (2300) is used for providing holes to the active region (2100); and the active region (2100) is used for realizing recombination of the holes and the electrons and emitting laser light. The laser (2000) further comprises a potential balance layer (2400), wherein the potential balance layer (2400) has a P-type doped structure, the potential balance layer (2400) is located on a P side of the active region (2100), the distance between the potential balance layer (2400) and the active region (2100) is less than or equal to 70 nm, and the potential balance layer (2400) is used for adjusting the position of a depletion region of the laser (2000), such that the depletion region of the laser (2000) coincides with the active region (2100).

Method to

Publication Number: WO2024/241751

Patent Applicant: Panasonic

The present invention is provided with: a multilayer structure which is formed on a nitride semiconductor substrate and comprises a 1st semiconductor layer containing a nitride semiconductor that has a 1st conductivity type, an active layer containing a nitride semiconductor that contains indium, and a 2nd semiconductor layer containing a nitride semiconductor that has a 2nd conductivity type; and a plurality of emitters which are formed in a stripe shape in the multilayer structure. The plurality of emitters emit light at a plurality of light emission wavelengths by photoluminescence, electroluminescence, or cathode luminescence. The plurality of light emission wavelengths have a distribution in which the plurality of light emission wavelengths become shorter from a 1st end of a laser diode bar in the arrangement direction of the plurality of emitters toward a specific portion other than the 1st end.



AA Top
BB Bottom
CC Surface temperature of wafer
DD Position within LD bar (arrangement direction)
EE In composition in active layer
FF Oscillation wavelength

ELECTRONICS

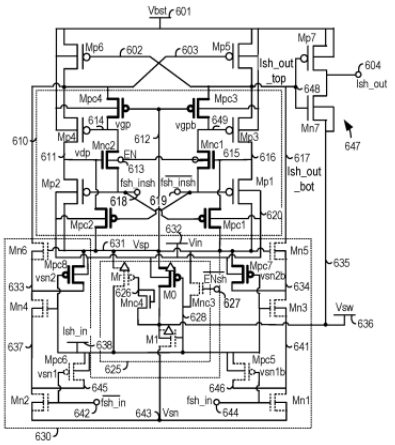
Notable new patent applications selected by Knowmade

Floating level shifter for DC-DC converter

Publication Number: US20240396552

Patent Applicant: Intel

Embodiments herein relate to a voltage converter with a floating level shifter. The floating level shifter is implemented on a silicon substrate using complementary metal-oxide semiconductor (CMOS) technology while the power train is implemented on a Gallium Nitride substrate. The floating level shifter may be all-digital and avoid the use of passive devices. The floating level shifter is responsive to a voltage output from a bootstrap circuit, a voltage of a switching node of a power train and a drive voltage of the bootstrap circuit, to shift an input signal to an output signal in a charge phase of a switching cycle. The output signal drives a high-side driver for a high-side transistor of the power train, where the voltage output from the bootstrap circuit and the voltage of the switching node alternate in charge and discharge phases of the switching cycle.

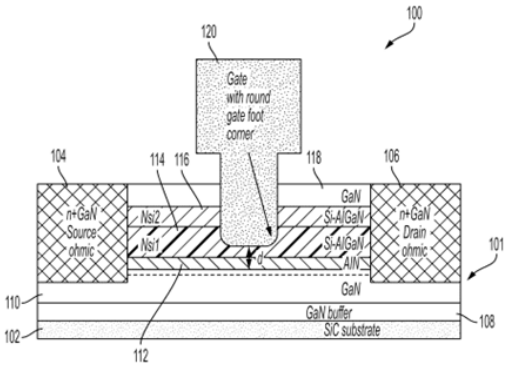


Recessed-gate HEMT with doped barriers and round gate foot corners

Publication Number: US20240379834

Patent Applicant: Teledyne Scientific & Imaging

A high electron mobility transistor comprising a substrate. The substrate comprising: a buffer layer, a channel layer disposed on the buffer layer, an interlayer disposed on the channel layer, a spacer layer, and a first barrier layer between the spacer layer and a cap layer, the spacer layer is between the interlayer and the first barrier layer. The high electron mobility transistor comprises a source electrode disposed on the channel, a drain electrode disposed on the channel, and a gate electrode disposed between the source electrode and the drain electrode, the gate electrode defining a longitudinal portion extending through the capping layer, wherein a distal end of the longitudinal portion is in contact with the first barrier layer defines an external fillet between the distal end and the longitudinal portion.

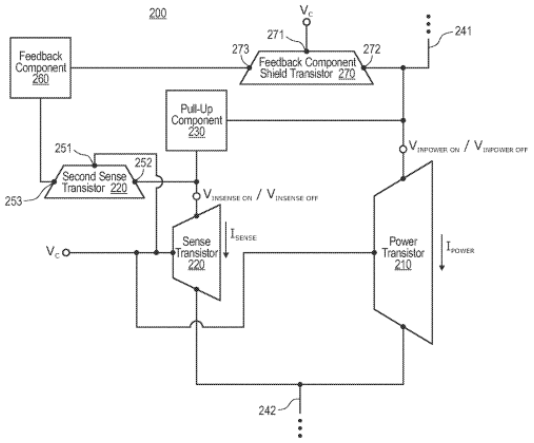


Current sensing by using aging sense transistor

Publication Number: US20240393374

Patent Applicant: Infineon

A current sense circuit that allows for accurate sensing of a power current that flows through a power transistor as the power transistor ages. The circuit includes the power transistor, a sense transistor and a pull-up component. The control nodes of the power transistor and the sense transistor are connected, causing the power transistor and sense transistor to be on or off simultaneously. The pull-up component is connected between the input node of the power transistor and the input node of the sense transistor. When power is provided to the pull-up component, and when each of the power transistor and sense transistor are off, the pull-up component forces a voltage present at the sense transistor input node to be approximately equal to a voltage present at the power transistor input node, causing the sense and power transistors to age together.

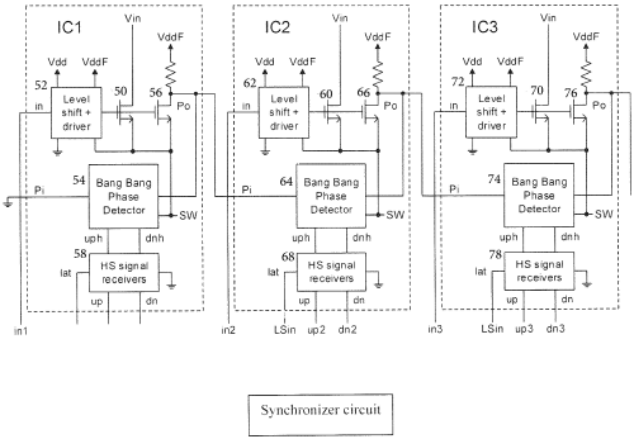


Synchronizing turn-on/turn-off times of parallel power FETs

Publication Number: US20240372545

Patent Applicant: EPC

A circuit for synchronizing the turn-on/turn-off times of parallel FETs. The circuit includes a plurality of integrated circuits and a synchronizer. Each of the integrated circuits includes a power FET which operates in parallel with the power FETs of the other integrated circuits, and a phase detector. The phase detector receives and compares the phase output signal of the integrated circuit with the phase output signal of another integrated circuit, and provides signals to the synchronizer regarding the relative turn-on times of the power FETs based upon the phase output signals. The synchronizer, in response to the signals from each of the integrated circuits, reduces or increases the turn-on times of the power FETs, thereby synchronizing the turn-on times of the power FETs.



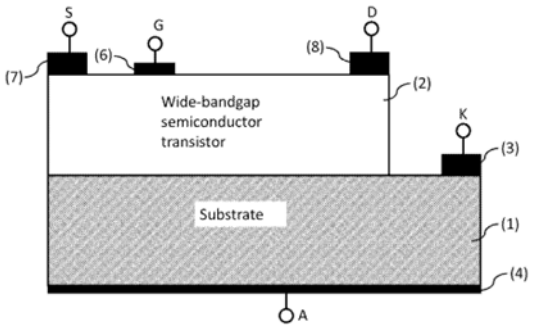
Synchronizer circuit

GaN power device using a diode incorporated in the substrate

Publication Number: US20240395632

Patent Applicant: Cambridge GaN Devices

A method of making a power device, the method comprising forming a substrate layer, wherein the substrate layer comprises a doped semiconductor material; forming a drift region of a high voltage diode in the substrate layer; forming a wide-bandgap semiconductor transistor over, and in physical contact with, a first section of a first surface of the substrate layer, wherein the first section includes at least part of the drift region of the high voltage diode; forming a first terminal over a second section of the first surface of the substrate layer; forming a second terminal over either: (i) a second surface of the substrate layer, wherein the second surface is opposite the first surface; or (ii) a third section of the first surface of the substrate layer; wherein the method comprises forming the drift region and the first and the second terminal such that a high voltage diode is formed in the substrate layer, wherein at least part of the diode is located below at least part of the wide-bandgap semiconductor transistor.

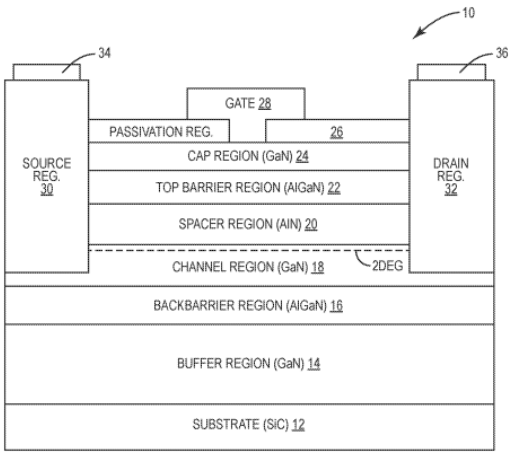


GaN-on-SiC FET with enhanced buffer and back barrier regions

Publication Number: US20240371992

Patent Applicant: Qorvo

A field effect transistor, such as a high electron mobility transistor, comprises a substrate, a buffer region, a back barrier region, a channel region, a source region, a drain region, and a gate contact. The buffer region is over the substrate and doped with a deep acceptor at a concentration in a range of 2×1016 cm−3 to 1×1018 cm−3. The back barrier region is over the buffer region and has a thickness in a range of 50 to 5000 Angstroms. The channel region is over the back barrier region. The source region and the drain region are arranged such that at least a portion of the channel region resides between the source region and the drain region. The gate contact is over the channel region and between the source region and the drain region.



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