

Hybrid Bonding

Patent Landscape Analysis – August 2024

Who are the key players and newcomers in the global IP race for the most advanced bonding technology shaping the future of semiconductor packaging?

REPORT OUTLINE

- Hybrid Bonding
- Patent Landscape Analysis
- August 2024
- PDF >70 slides
- Excel file >1,600 patent families
- Reference: KM24003
- 4,990 EUR for a multi-user license



KEY FEATURES

- **Global patenting trends**, including time evolution of patent publications, countries of patent filings, etc.
- **Main patent assignees and IP newcomers** in the different segments.
- Key players' **IP position** and the relative **strength** of their patent portfolio.
- Patents categorized by **type of invention** (manufacturing methods, equipment, semiconductor structures and devices) and **targeted applications** (image sensors, 2.5D/3D IC, 3D-stacked memories, photonics, etc.)
- **IP profile of key players** (patent portfolio overview, technical coverage, geographical coverage, key patents, recent IP activity, etc.)
- **Excel database** containing all patents analyzed in the report, including **patent segmentations** and hyperlinks to an **updated online database**, along with the **complete data by assignee** from the statistical analyses.

RELATED REPORTS & MONITORS

- [Advanced Semiconductor Packaging – Patent Monitor \(subscription\)](#)
- [Hybrid Bonding – Patent Landscape 2019](#)

Hybrid bonding has become a key enabler of advanced packaging

Hybrid bonding combines dielectric-to-dielectric and metal-to-metal bonds to interconnect wafer-to-wafer, die-to-wafer, or die-to-die without the need for solder or other adhesives. This bonding technology is used for the vertical stacking of multiple chips, enabling 3D heterogeneous integration and interoperability of different types of chips with various functions (e.g., logic, memory, analog, sensors) within a single package. **Hybrid bonding** enables finer pitch (<10µm, or even <1µm) with significant benefits for interconnect density and device performance. The direct metal-to-metal contact facilitates efficient heat dissipation and reduces the parasitic delay. The dielectric insulates each metal pad so that there is no signal interference between the pads.

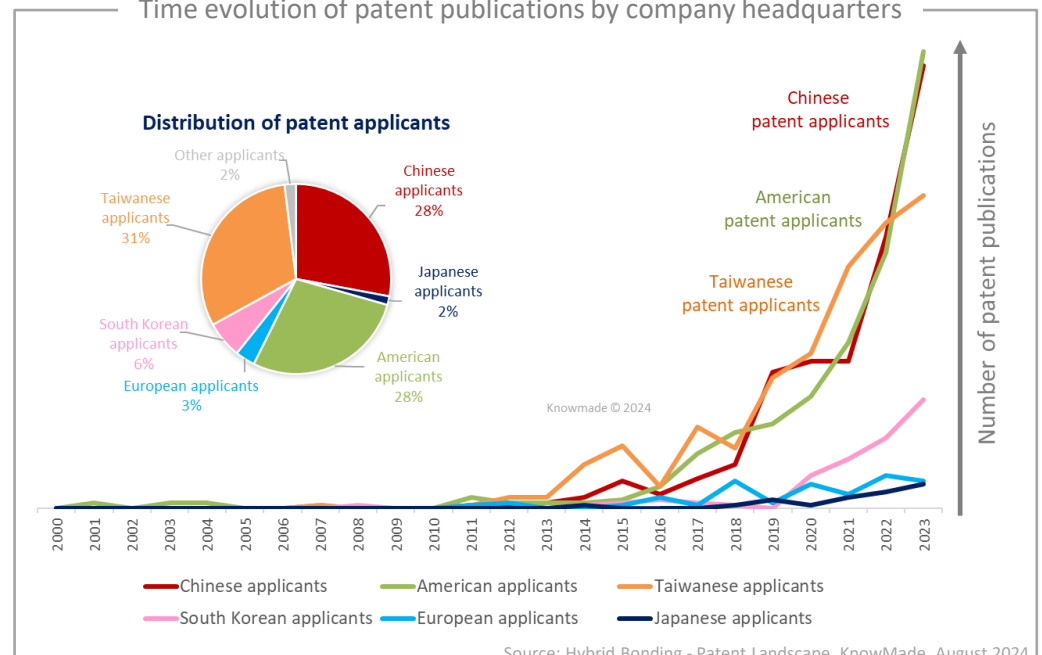
Hybrid bonding technology emerged in 2005 with the introduction of **Ziptronix's** direct bond interconnect (DBI®) technology. In 2015, **Tessera** (now **Adeia**) acquired **Ziptronix**, and DBI® technology entered the market in 2016 through Sony's CMOS image sensor (CIS) used in Samsung's Galaxy S7 mobile phone. Since then, **hybrid bonding** technology has been explored for various applications, including memory, logic, RF, and photonics, and it is now being adopted by more companies across the semiconductor industry.

Over the past five years, **hybrid bonding** technology has become a key enabler of advanced semiconductor packaging, leading to a strong increase in patenting activity and a significant evolution of the competitive intellectual property (IP) landscape. Major patent owners have strengthened their IP positions in the US, China, and Europe, while various new players have entered the patent landscape. It is now crucial for companies operating in the semiconductor packaging industry to closely examine hybrid bonding technology from an IP perspective.

In this context, **Knowmade is releasing a new patent landscape report** focusing on the hybrid bonding process and semiconductor devices made using hybrid bonding interconnects. Over **5,800 patents** from more than **1,600 patent families** (inventions) have been selected. This report aims to provide insights into current IP activities, the positions of key IP players, the applications they target in their patents, and how their patent portfolios can support their market strategies.

Hybrid Bonding Patent Landscape

Time evolution of patent publications by company headquarters



Understanding the main trends, the key players' IP position and IP strategy

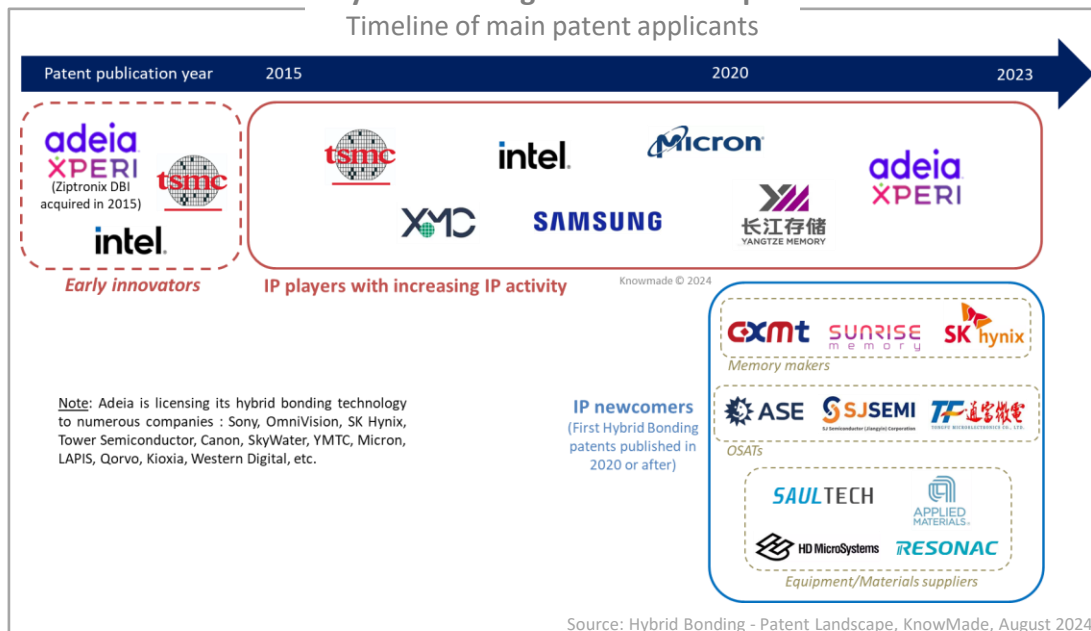
Through patent analysis, we describe the position of IP players, unveil their strategies to strengthen their IP portfolio, highlight their capability to limit the patenting activity and freedom-to-operate of other firms, identify promising new players, and forecast what would be the future IP leaders. IP competition analysis should reflect the vision of players with a strategy to enter and develop their business in the **advanced semiconductor packaging** market. In this report, we provide a comprehensive overview of the competitive IP landscape and latest technological developments related to **hybrid bonding** technology. The report covers **IP dynamics** and **key trends** in terms of patents applications, patent assignees, filing countries, patented technologies, and targeted applications. It also identifies the **IP leaders**, most **active patent applicants**, and sheds light on **under-the-radar companies and new players** in this field.

Invention type, targeted applications, and key patents

The patents have been categorized according to the **type of claimed invention** (hybrid bonding manufacturing methods and interface engineering, equipment for hybrid bonding technology, hybrid bonded semiconductor structures or devices) and the **applications mentioned in the patents** (image sensors, 2.5D/3D ICs, 3D-stacked memories, photonics, MEMS, RF, etc.). The 2.5D/3D IC segment is currently driving patenting activity, while patents related to other applications, such as photonics, microLED, MEMS, and RF, have surged.

Hybrid Bonding Patent Landscape

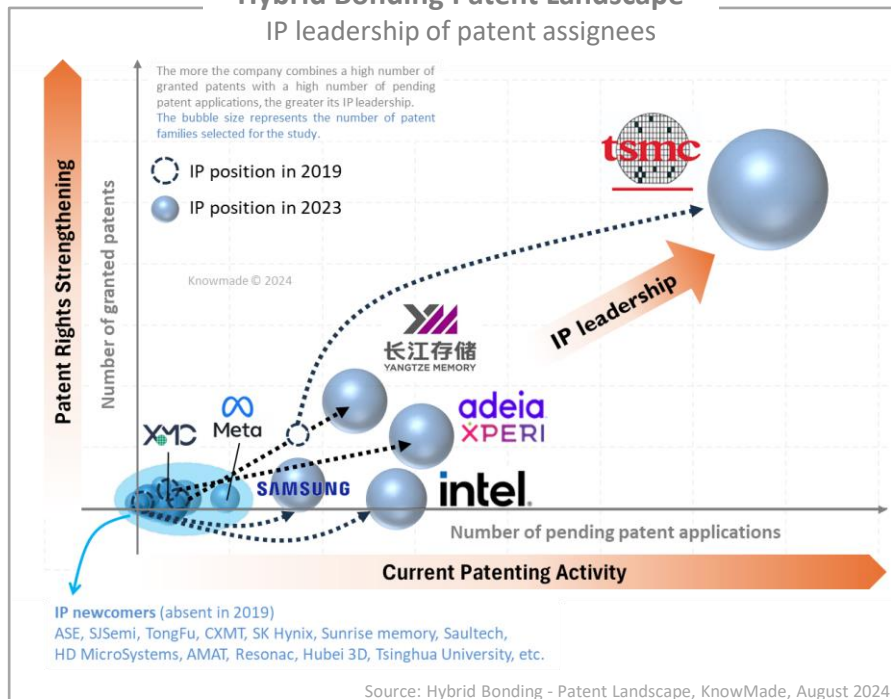
Timeline of main patent applicants



Among the 1,600+ inventions studied in this report, we have identified **over 280 key patents** that are most critical in terms of prior art, IP risks, and technology. The report provides their patent owners and the technical/application segments to which they belong.

Hybrid Bonding Patent Landscape

IP leadership of patent assignees



A dynamic IP landscape: evolution of leading players' positions and entry of new patent applicants

TSMC, Adeia, YMTC, Intel, and Samsung are leading the **patent landscape**, increasing patenting activity, and expanding invention protection in key countries. As pioneer and owner of DBI® technology, Adeia has adopted an aggressive strategy to assert its patents and license its hybrid bonding IP portfolio to various semiconductor companies, including **Sony, YMTC, Micron, and Kioxia**. Despite its strong IP position, other players have been developing their own hybrid bonding patent portfolios. In recent years, more memory makers have become involved in the IP landscape (CXMT, SK Hynix, Sunrise Memory), and OSATs and equipment/materials suppliers have entered the IP arena (ASE, TongFu, SJSemi, Applied Materials, Saultech, HD MicroSystems). In this report, we provide an overview of the IP portfolios held by key players and describe **key patents** and **recent IP activities**. Additionally, we highlight the main **IP collaborations** (co-owned patents, IP transfers, licensing agreements) and **patent litigations**.

Useful Excel patent database

This report includes an extensive **Excel database with** all patents analyzed in this study, including **patent information** (numbers, dates, assignees, title, abstract, etc.) and **hyperlinks to an updated online database** (original documents, legal status, etc.), **affiliation segments** (manufacturing methods, equipment, semiconductor devices, image sensors, 2.5D/3D IC, 3D-stacked memory, etc.), and **key patents**. Additionally, the Excel file comprises the **complete data by assignee** from the statistical analyses, including the number of patent families, timeline of patenting activity, number of granted patents and pending patent applications, and geographical coverage of patent portfolio.



Companies mentioned in the report (non-exhaustive)

TSMC, YMTC, Xperi/Adeia, Intel, Samsung, XMC, Micron, Tongfu Microelectronics, ASE, Meta (Facebook), Nanya Technology, CXMT, Huawei, Onsemi, OmniVision, AMD, ICLeague Technology, Monolithic 3D, UMC/Wavetek, Qualcomm, SJSemi, Saultech, SK Hynix, Tsinghua University, CEA, imec, Galaxycore Microelectronics, Apple, EVG, HD MicroSystems, NCAP, STMicroelectronics, Applied Materials, Resonac, GlobalFoundries, SunRise Memory, Alibaba Group, AP Memory, SMIC, Powerchip Semiconductor Manufacturing, MICLEDI, AMS-Osram, SmartSens Technology, Shenzhen Aoshiwei Technology, MediaTek, IBM, RTX Corporation, pSemi, Winbond electronics, Sony, NVIDIA, Haiguang Information Technology, Shanghai Huali Integrated Circuit Manufacturing, JCET Group, SEMES, Tectus Group, Hanmi, Western Digital, Shibaura Mechatronics, Ningbo Semiconductor International Corporation (NSI), HIDM - Huaian Imaging Device Manufacturer, Bruker, Suzhou Ultiview Technology, KLA, Shanghai Fudan Microelectronics Group, Anhui Xinbiyou Information Technology, Tokyo Electron, Shanghai Yibu Semiconductor, HTSI, GROQ, Dixtech innovation, Qingdao New Core Technology, PsiQuantum, Canon, Infineon, Shanghai Biren Intelligent Technology, Yangtze River Advanced Storage Industry Innovation Center, G-ray Switzerland, and more.

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- Scope of the report
- Reading guide
- Excel database

EXECUTIVE SUMMARY **11****EXCEL DATABASE**

Excel file that includes all patent selected for this study, along with the complete data by assignee from the statistical analyses.

PATENT LANDSCAPE OVERVIEW **20**Main trends and IP players **21**

- Time evolution of patent publications
- Main patent assignees
- Timeline of IP players
- Typology of main IP players
- IP newcomers
- Current legal status of main players' patents
- IP leadership of patent assignees and evolution from 2019
- Geographical coverage of main players' patents

Main IP collaborations **34**

- Co-owned IP
- IP transfers
- Licensing agreements

Patent segmentation **38**

- Segments definition
- Type of claimed invention:
 - Hybrid bonding manufacturing process and interface engineering

- Apparatus/Equipment for hybrid bonding
- Semiconductor structure or device made using hybrid bonding interconnects
- Targeted applications
 - Image sensor (SPADs, CMOS image sensors, light sensing devices, etc.)
 - 2.5D/3D IC (assembly of any type of IC dies, excluding memory-on-memory)
 - 3D-stacked memory (memory-on-memory)
 - Other applications (RF, MEMS, Photonics, LEDs, etc.)
- Time evolution of patent publication by segment
- Main patent assignees by segment
- IP leadership of patent assignees for each segment

KEY PATENTS **48**

- Most important patents in terms of prior-art, IP risks and technology
- Segments to which key patents belong
- Owners of key patents

IP PROFILE OF A SELECTION OF PATENT ASSIGNEES **52**

TSMC, Adeia/Xperi, TongFu, ASE

For each player:

- Patent portfolio overview (IP dynamics, segments, legal status, geographic coverage, etc.)
- Description of key patents
- Description of recent patent applications

PATENT LITIGATION **67****ANNEX** **70**

- Methodology for patent search, selection and analysis
- Methodology to identify key patents
- Terminology

KNOWMADE PRESENTATION **76****AUTHORS****Dr. Pauline Calka**

Pauline works for Knowmade as a patent analyst in the fields of semiconductor manufacturing and advanced packaging. She holds a PhD in Memory from the University of Grenoble Alpes (France), in partnership with the CEA-Leti (France). After an Alexander von Humboldt Postdoc fellowship position at the Technical University of Berlin (Germany) and the Leibniz Institute for High Performance Microelectronics on ReRAM development, Pauline worked five years at ASM International (Belgium) as Senior Process Engineer on thin film development for logic, memory and MEMS, and two years at CEA-Leti as Integration Engineer on imaging CMOS sensors.

Contact: pauline.calka@knowmade.fr

**Dr. Nicolas Baron**

Nicolas is CEO and co-founder of Knowmade. He manages the development and strategic orientations of the company and personally leads the Semiconductor department. He holds a PhD in Physics from the University of Nice Sophia-Antipolis, and a Master of Intellectual Property Strategies and Innovation from the European Institute for Enterprise and Intellectual Property (IEEPI) in Strasbourg, France.

Contact: nicolas.baron@knowmade.fr

ABOUT KNOWMADE

KnowMade is a technology intelligence and IP strategy consulting company specialized in analyzing patents and scientific publications. The company helps innovative companies, investors, and R&D organizations to understand competitive landscape, follow technological evolutions, reduce uncertainties, and identify opportunities and risks in terms of technology and intellectual property.

KnowMade's analysts combine their strong technology expertise and in-depth knowledge of patents with powerful analytics tools and methodologies to turn patent information and scientific literature into actionable insights, providing high added value reports for decision makers working in R&D, innovation strategy, intellectual property, and marketing. Our experts provide prior art search, patent landscape analysis, freedom-to-operate analysis, IP due diligence, and monitoring services.

KnowMade has a solid expertise in Compound Semiconductors, Power Electronics, Batteries, RF Technologies & Wireless Communications, Solid-State Lighting & Display, Photonics, Memories, MEMS & Sensors, Semiconductor Packaging, Medical Devices, Medical Imaging, Microfluidics, Biotechnology, Pharmaceuticals, and Agri-Food.

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Patent Landscape Analysis – August 2024

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Definitions

“Acceptance”: Action by which the Buyer accepts the terms and conditions of sale in their entirety. It is done by signing the purchase order which mentions “I hereby accept KnowMade’s Terms and Conditions of Sale”.

“Buyer”: Any business user (i.e. any person acting in the course of its business activities, for its business needs) entering into the following general conditions to the exclusion of consumers acting in their personal interests.

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“Intellectual Property Rights” (“IPR”) means any rights held by the Seller in its Products, including any patents, trademarks, registered models, designs, copyrights, inventions, commercial secrets and know-how, technical information, company or trading names and any other intellectual property rights or similar in any part of the world, notwithstanding the fact that they have been registered or not and including any pending registration of one of the above mentioned rights.

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1. Scope

1.1 The Contracting Parties undertake to observe the following general conditions when agreed by the Buyer and the Seller. Any additional, different, or conflicting terms and conditions in any other documents issued by the buyer at any time are hereby objected to by the seller, shall be wholly inapplicable to any sale made hereunder and shall not be binding in any way on the seller.

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BIC or SWIFT code: CCBPFRPPMAR

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3.3 Payment is due by the Buyer to the Seller within 30 days from invoice date, except in the case of a particular written agreement. If the Buyer fails to pay within this time and fails to contact the Seller, the latter shall be entitled to invoice interest in arrears based on the annual rate Refi of the «BCE» + 7 points, in accordance with article L. 441-6 of the French Commercial Code. Our publications (report, database, tool...) are delivered only after reception of the payment.

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b) any claim attributable to errors, omissions or other inaccuracies in the Product or interpretations thereof.

4.4 All the information contained in the Products has been obtained from sources believed to be reliable. The Seller does not warrant the accuracy, completeness adequacy or reliability of such information, which cannot be guaranteed to be free from errors.

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