PATENT MONITOR

Advanced Packaging

Quarterly Report

Q4 2022

SAMPLE

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Patent & Technology Intelligence

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PLAYERS IP ACTIVITY DURING THE QUARTER 24

Pure play foundries 25
- *TSMC*
- *GlobalFoundries*

OSATs 29
- *Amkor*
- *ASE*
- *SPIL*
- *JCET*
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- *Powertech Technology*
- *Deca*
- *Huatian Technology*
- *SJSemi*
- *Tongfu Microelectronics*

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- *Samsung*
- *Infineon*
- *Intel*
- *Micron*
- *SK Hynix*
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ANNEX 50

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INTRODUCTION & METHODOLOGY

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INTRODUCTION
Context

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2.5D/3D stacking and fan-out WLP are promising solutions to meet the needs of the semiconductor packaging market.
It is crucial to monitor patent activity and IP strategies of key semiconductor packaging players.

In the semiconductor industry, there is a growing demand for integrating more compute and memory within a single package in order to achieve smaller form factors and improve product performance. However, Moore's Law becomes increasingly difficult to achieve as node advancement reaches its limits. As a result, the process of chip miniaturization has been slowing down. **Advanced packaging techniques**, such as **2.5D & 3D stacking**, and **fan-out wafer level packaging**, have emerged as crucial solutions to meet the needs of the semiconductor industry. These new approaches allow for the integration of multiple dies into a single package, with the possibility of combining mature and advanced nodes, and they have supplemented the dominant flip-chip (FC) and wire-bond (WB) technologies. The roadmap for these **advanced packaging technologies** is challenging and the supply chain is becoming increasingly competitive, with the demand for high-density fan-out (HD FO) redistribution layers (RDLs), high-density input/output interconnections (I/O), and advanced interconnect technologies such as silicon interposer, embedded bridge, hybrid bonding, and chiplets approach.

The market for **2.5/3D packaging** shows the most potential for growth, with 3D SoC technology growing the most driven by the increasing popularity of hybrid bonding for chiplets 3D integration. In the fan-out WLP industry, the segment experiencing the highest growth is the ultra-high density fan-out (UHD FO), which has emerged as a more cost-effective solution compared to silicon interposers. Semiconductor packaging was primarily performed by OSATs such as **ASE/SPIL**, **Amkor**, **JCET**, etc. and they continue to play an important role in this field. However, it is **TSMC**, **Samsung** and **Intel** that have been developing innovative 2.5D/3D packaging solutions such as silicon interposer, embedded bridge, and hybrid bonding. By offering advanced back-end solutions and using their front-end capabilities, these companies poised to influence future technology and intellectual property (IP) developments in this area.

In this context, it is crucial to monitor patent activity and intellectual property (IP) strategies of key players. Such knowledge can assist in understanding your competitors’ R&D roadmap and strategies, evaluate the risks, and detect business opportunities.

The **Advanced Packaging Patent Monitor** gives periodic insights on the IP activity of a selection of key companies: **TSMC**, **Intel**, **Samsung**, **Amkor**, **ASE**, **SPIL**, **JCET**, **Deca**, **Nepes**, **Powertech (PTI)**, **SJSemi**, **Tongfu (TFME)**, **Huatian**, **Infineon**, **Micron**, **SK Hynix**, **YMTC**, **GlobalFoundries**, and **Xperi/Adeia**.

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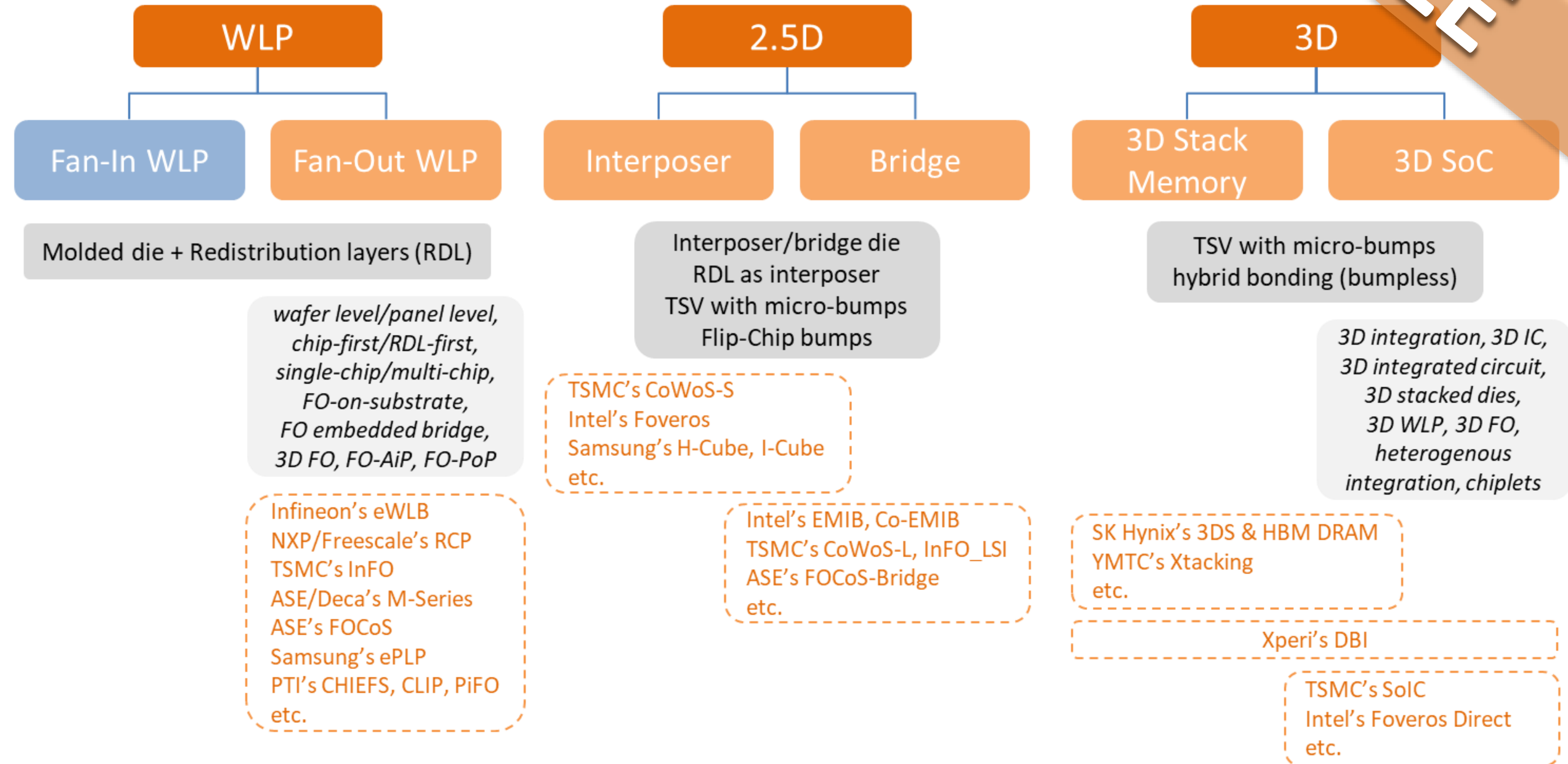
INTRODUCTION

Scope of the patent monitoring service



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INTRODUCTION

Methodology and segment definition

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- The data are extracted from the **FamPat worldwide patent database** (ORBIT Intelligence) which provides 100+ million patent documents from 100 patent offices (USA, Japan, Europe, China, Korea, Taiwan, Hong Kong, Singapore, etc.).
- Patent families are manually segmented into **three main categories of advanced packaging** (fan-out WLP/PLP packaging, 2.5D & 3D integration, other packaging) and **different sub-segments** (Si interposer, Si bridges, hybrid bonding, etc.). A patent family can belong to multiple technical or sub-segments.
- Three types of patents are selected: **new patent families** (i.e., new inventions), **patent families granted for the first time**, and **patents newly expired or abandoned**.
- Four types of legal events are monitored: **US litigations**, **European oppositions**, **IP collaborations** (i.e., patent co-filings), and **transfer of IP rights** (i.e., change in patent ownership).

TECHNICAL SEGMENTATION

Fan-out packaging (FO)
- Wafer level packaging (FO-WLP)
- Panel level packaging (FO-PLP)

Includes Fan Out 2.5D/3D and Fan Out Package-on-Package (FO-PoP)

2.5D/3D IC (heterogeneous integration, chiplets)
- Interposer/bridge (silicon interposer, embedded interconnect bridge)
- Hybrid Bonding (i.e., direct metal-to-metal and oxide-to-oxide bonding without bumps)
- 3D-stacked memory (excludes multiple single memory cells fabricated on a same wafer)

Others

Includes
- Traditional packaging (flip-chip, fan-in, chip scale packaging, SoC, etc.)
- Packaging that consists of a combination of several packages (Package-on-Package). Note that Fan-Out PoP is included in Fan-Out packaging segment
- FAB equipment and materials that may be used in packaging
- Data processing / computing enabled by multiple packaged electronics components

LEGAL STATUS

New patent families
Patent family published for the first time during the quarter

New granted patent families
Patent family granted for the first time during the quarter

New dead patents
Patents expired or abandoned (revoked, lapsed) during the quarter

LEGAL EVENT

Patent litigation (US) and **oppositions** (Europe)
IP collaborations (i.e., patent co-filed by different entities)
Transfer of IP rights (i.e., change in patent ownership) when data are available

Technical segments will be adapted over time according to the technological evolution of advanced packaging

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INTRODUCTION

Companies tracked in this patent monitor

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OSAT
Outsourced Semiconductor Assembly and Test companies

- Amkor Technology — *Includes J-Devices and Nanium*
- ASE, SPIL — *Members of **ASE Technology Holding***
- DECA
- JCET
- nepes — *Includes subsidiary **Nepes Laweh***
- Powertech Technology Inc. — *Includes Nepes Pte. Ltd. Singapore acquired in 2014*
- HUA TIAN 华天科技（昆山）电子有限公司 HUATIAN TECHNOLOGY(KUNSHAN)ELECTRONICS CO.,LTD
- SJSEMI — *Joint venture **SMIC / JCET** founded in 2014*
- TF 通富微電 Tongfu Microelectronics

Pure play foundries
Manufacturers that makes chips for other companies

- tsmc
- GlobalFoundries™

IDM
Integrated Device Makers

- intel
- infineon
- SAMSUNG
- Micron
- SK hynix
- YANGTZE MEMORY

Memory makers (Samsung, Micron, SK hynix, Yangtze Memory)

NPE
Non-practicing entities

- XPERI — *Includes Adeia, Invensas, Tessera, …*

Company selection could be adapted over time according to the ecosystem evolution of advanced packaging

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PATENT MONITOR

Take advantage of quarterly updates on IP activities

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CONTENTS

Quarterly IP database (Excel file)

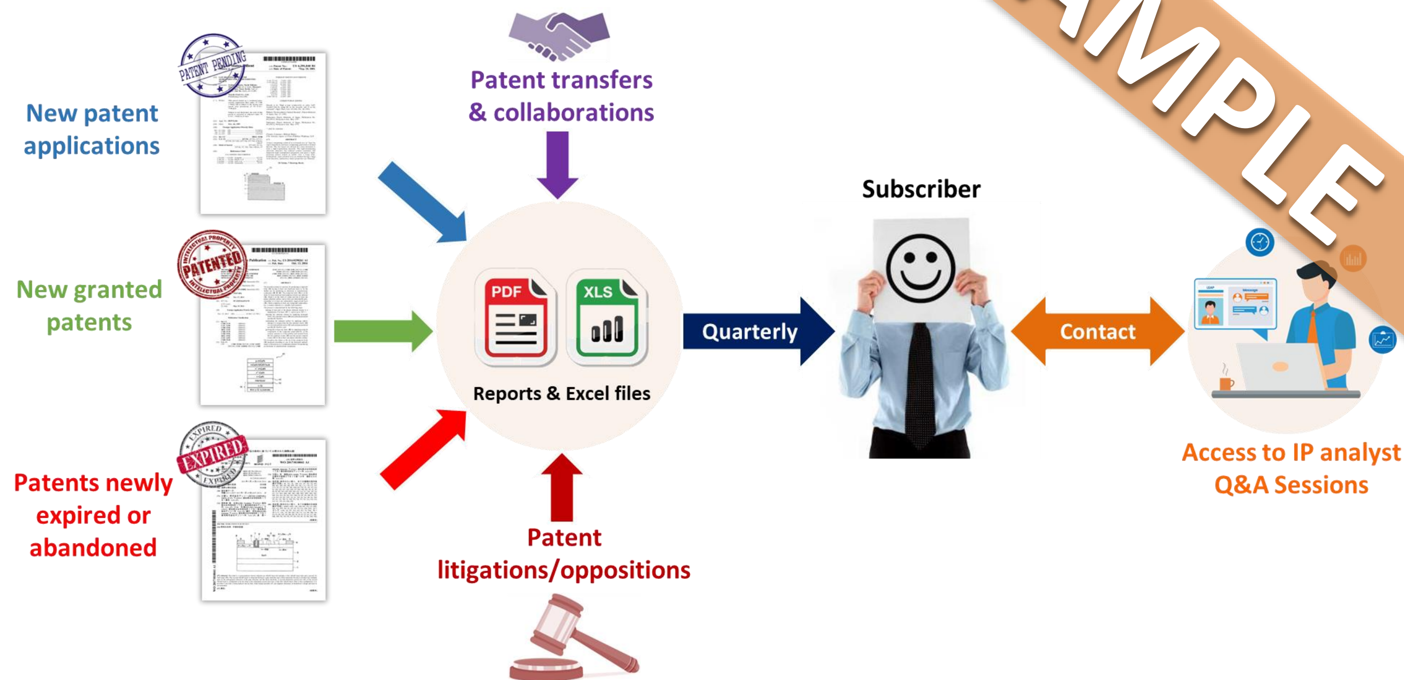
- New patent families (inventions)
- Patent families granted for the first time
- Patents newly expired or abandoned
- Transfer of IP rights (re-assignment, licensing)
- Patent litigations and oppositions
- Patents categorized by technology, supply chain segment, application, etc.

Quarterly IP report (PDF slide deck)

- Key fact & figures of the quarter
- Graphs and comments covering the patent landscape evolutions
- A close look at the key IP players, newcomers, and key patented technologies

Access to IP analyst (100h per year)

- Q&A session and discussion with our IP analysts regarding the quarterly report results, trends, analyses, specific patented technologies or companies' patent portfolios in the field of the patent monitor.



WHY YOU SHOULD SUBSCRIBE

- ✓ Track your **competitors**, partners or clients
- ✓ Identify **newcomers** to your technology field
- ✓ Early detect **opportunities** and risks for your business strategy
- ✓ Be ahead of **technology trends**
- ✓ Identify emerging research areas and **cutting-edge technology** developments
- ✓ Mitigate patent **infringement risks**
- ✓ Take advantage of **free technologies**

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PATENT MONITOR

Quarterly report

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On a quarterly basis, this report will provide the IP trends over the last three months, with a close look to key patented technologies from a selection of key players:

TSMC, Intel, Samsung, Amkor, ASE, SPIL, JCET, Deca, Nepes, Powertech Technology, SJSemi, TFME, Huatian, Infineon, Micron, SK Hynix, YMTC, GlobalFoundries, Xperi

New patent applications
New granted patents
Patents newly expired or abandoned
Patent transfers & collaborations
Reports & Excel files
Patent litigations/oppositions

	Q4 2022	Fan Out Packaging		2.5D/3D Integration				Others
		All fan-out packaging (WLP & PLP)	Fan out panel level packaging (FOPLP)	All 2.5D/3D packaging technologies	Interposer / Bridge	Hybrid bonding	3D stacked memory	
New patent families (inventions)	963	101	9	340	276	59	105	564
Patent families newly granted	583	65	3	175	138	36	47	371
Patents expired or abandoned								
IP collaborations (patent co-filings)								
IP transfers (change in ownership)								
US litigations								
EU oppositions								

Samsung Group
Q4-2022 IP ACTIVITY

	Q4 2022	Fan-out	FO - Panel level	2.5D/3D	Interposer Bridge	HB	Stacked 3D memory	Others
New patent families (inventions)	205	30	8	76	61	6	27	111
Patent families newly granted								
Patents expired or abandoned								

ASE
Q4-2022 IP ACTIVITY

	Q4 2022	Fan-out	FO - Panel level	2.5D/3D	Interposer Bridge	HB	Stacked 3D memory	Others
New patent families (inventions)	64	4		9	9			52
Patent families newly granted								
Patents expired or abandoned								

YMTC
Q4-2022 IP ACTIVITY

	Q4 2022	Fan-out	FO - Panel level	2.5D/3D	Interposer Bridge	HB	Stacked 3D memory	Others
New patent families (inventions)	25	1		2		2		22
Patent families newly granted	6			1		1		5
Patents expired or abandoned								

YMTC signed a license agreement with Xperi

- ✓ Main patent applicants, their notable patent filings and technologies.
- ✓ New entrants and their patents.
- ✓ Technology trends and notable patented technical solutions.
- ✓ Key patents newly granted, their owners and claimed inventions.
- ✓ Main IP right transfers (reassignments, licensing agreements).
- ✓ Key patents newly expired or abandoned, their owners and their potential market impact.
- ✓ Noteworthy news on patent litigation and opposition, plaintiffs and defendants, patents and products involved.

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PATENT MONITOR

Quarterly IP database

Segments
(an X indicate a patent belonging to the segment)

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Questel unique family ID (FAN)	Current assignees of the patent family	Re-assignments	Publication numbers of the patent family	Title	Abstract	Claims	Current legal status of the patents	Earliest publication date of the patent family	Earliest grant date	Expected expiry date	Biblio summary (link to updated online database)
103771997	TAIWAN SEMICONDUCTOR	CHANG, JEN-YUAN; FROM 2022-05-31	US20230052136	Thermoelectric	An integrated circuit	What is claimed is:	PENDING	2022-12-13		2042-06-07	Open
103770513	TAIWAN SEMICONDUCTOR	LIN, HSIANG-WEI; FROM 2021-12-08 TO	US20230048536	Interconnect with	A method includes	What is claimed is:	PENDING	2022-12-13		2042-01-03	Open
103769814	TAIWAN SEMICONDUCTOR	WANG, MENG-HAN; FROM 2022-06-20	DE102022118524	Backside	The present	1. A structure,	PENDING	2022-12-09		2042-06-29	Open
103687839	TAIWAN SEMICONDUCTOR	CHANG, JEN-YUAN; FROM 2022-01-18 TO	US20230041839	Hybrid Node Chiplet	The present	What is claimed is:	PENDING	2022-12-06		2042-05-24	Open
103620749	TAIWAN SEMICONDUCTOR	LAI, TEN LIAN; FROM 2022-04-11 TO	US20230036280	Seal Ring Structure	The present	What is claimed is:	PENDING	2022-12-16	2022-12-16	2042-05-05	Open
103618124	TAIWAN SEMICONDUCTOR	LEE, CHIEH; FROM 2021-11-22 TO 2021-11-	DE102022102731	Dram computation	A memory circuit	1. A memory circuit	PENDING	2022-11-22		2042-01-31	Open
103530388	TAIWAN SEMICONDUCTOR	CHENG, CHIH-CHANG; FROM	KR10-2023-0015830	Semiconductor	The present	What is claimed is:	PENDING	2022-12-06		2042-01-07	Open
103529025	TAIWAN SEMICONDUCTOR	PENG, CHI-CHUN; FROM 2022-01-27	US20230023353	Semiconductor die	A die dipping	What is claimed is:	PENDING	2022-11-22		2042-02-22	Open
103528982	TAIWAN SEMICONDUCTOR	PRIYA; FROM 2022-	US20230023268	Dicing Process in	A method includes	What is claimed is:	PENDING	2022-11-25		2042-03-15	Open
103422764	TAIWAN SEMICONDUCTOR	CHIOU, WEN-CHIH; FROM 2022-04-28	US20230021005	Semi			PENDING	2022-12-20	2022-12-20	2042-05-06	Open
103420378	TAIWAN SEMICONDUCTOR	CHEN, CHIH-HAO; FROM							2023-05-21	2042-03-04	Open
103324632	TAIWAN SEMICONDUCTOR	FROM 2022-01-17 TO	KR10-2023-0007929	Integrated 3DIC With	A method includes	What is claimed is:	PENDING	2022-10-28		2042-01-19	Open
103324429	TAIWAN SEMICONDUCTOR	WU, CHENG-HSIEN; FROM 2021-08-16 TO	US20230011752	Local interconnect	Semiconductor	What is claimed is:	PENDING	2022-11-11		2041-10-07	Open
103323778	TAIWAN SEMICONDUCTOR	PAN, PHILEX MING-YAN; FROM 2022-01-	KR10-2023-0009810	Method of	A system includes: a	1. A system for	PENDING	2022-11-01		2042-02-24	Open
103323526	TAIWAN SEMICONDUCTOR	CHO, CHENG-I; FROM 2021-09-10 TO	US20230010038	Wafer Bonding	Wafer bonding	What is claimed is:	PENDING	2022-11-04		2041-09-10	Open
103254483	MICRON TECHNOLOGY		CN218182211	Semiconductor	The utility model	1. A semiconductor	(CN218182211UU) GRANTED	2022-12-30	2022-12-30	(CN218182211UU) 2032-07-08	Open
103251801	LINQU SAMSUNG ELECTRONICS		CN115535387	Package	The invention	1. The utility model	(CN115535387A) PENDING	2022-12-30		(CN115535387A) 2042-10-09	Open
103247897	HUATIAN TECHNOLOGY		CN115547970	Silicon-based gallium	The invention	1. The utility model	(CN115547970A) PENDING	2022-12-30		(CN115547970A) 2042-10-11	Open
103240708	INTEL		CN115551121	Apparatus and	The present	1. An apparatus,	(CN115551121A) PENDING	2022-12-30		(CN115551121A) 2042-06-20	Open
103239348	CHANGDIAN INTEGRATED		CN218182174	Wafer warping	The utility model	1. The utility model	(CN218182174UU) GRANTED	2022-12-30	2022-12-30	(CN218182174UU) 2032-08-30	Open
103238465	ADVANCED SEMICONDUCTOR		CN218183493	(CN218183493U) Earphone assembly	The utility model	1. An earphone	(CN218183493UU) GRANTED	2022-12-30	2022-12-30	(CN218183493UU) 2032-08-22	Open
103237482	ADVANCED SEMICONDUCTOR		CN115548003	Semiconductor	The invention relates	1. A semiconductor	(CN115548003A) PENDING	2022-12-30		(CN115548003A) 2041-06-30	Open

Questel unique family ID (FAN)	REASON OF SELECTION: New inventions	New granted patent families	Expired patents	Patent transfers	Patent litigations	Fan Out Packaging: All fan-out packaging (wafer level & panel level)	Fan out panel level packaging (FOPLP)	2.5D/3D: All 2.5D/3D packaging technologies	Interposer / Bridge	Hybrid bonding	3D st... me...	Others
103771997	x							x	x	x		
103770513	x											x
103769814	x											x
103687839	x							x	x			
103620749	x											x
103618124	x							x	x			
103530388	x							x	x			
103529025	x							x	x		x	
103528982	x					x		x	x			
103422764	x							x	x	x		
103420378	x											
103324632	x							x		x		
103324429	x											x
103323778	x							x			x	
103323526	x							x		x		
103254483	x											x
103251801	x											x
103247897	x											x
103240708	x											x
103239348	x					x						x
103238465	x											x
103237482	x											x

INTRODUCTION | **Q4 2022 IP activity**

Patent information
(Assignees, numbers, dates, title, abstract, claims, legal status, hyperlink to updated online database)

Identify easily and efficiently
- New patents applications
- Patents newly granted
- Patents expired or abandoned
- Transfer of IP rights
- Patent litigation

Patent segmentation

The patents are **manually categorized in technical segments** using keyword analysis of patent title, abstract and claims, in conjunction with expert review of the subject-matter of inventions.

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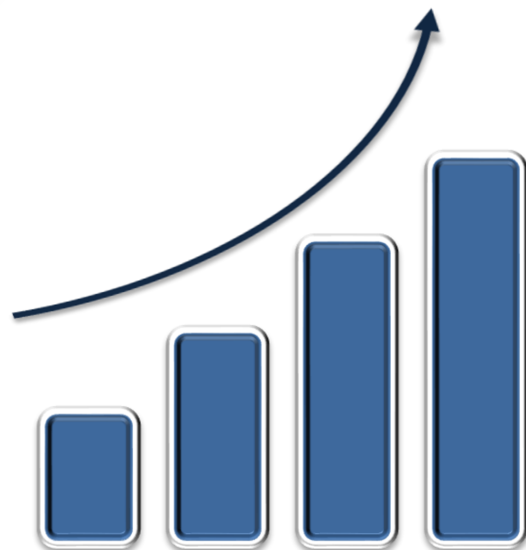

MAIN TRENDS

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MAIN TRENDS

Fan-Out wafer/panel level packaging

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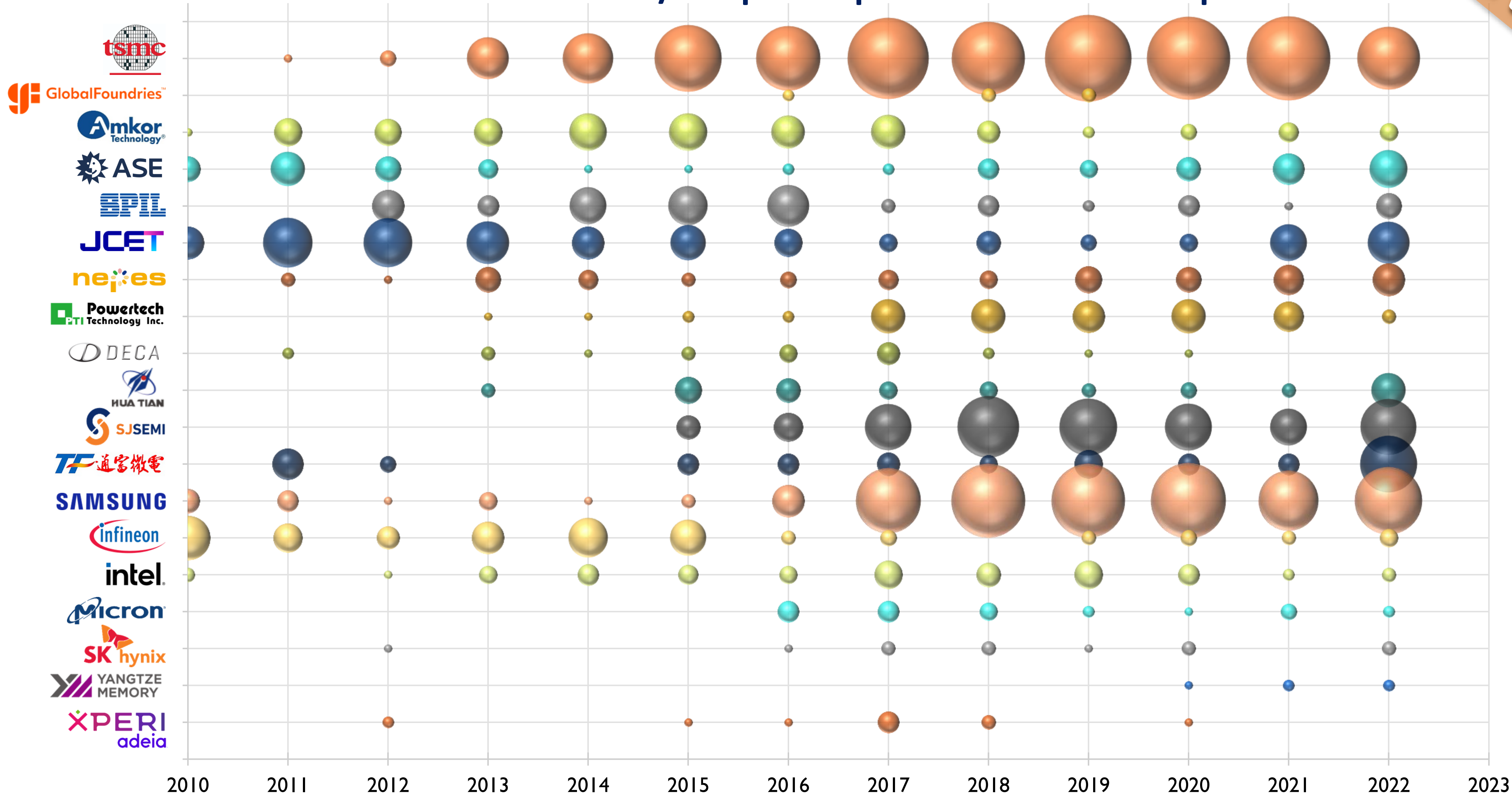

Bubble size is related to the number of patent families (inventions). A patent family is a set of patents filed in multiple countries to protect a single invention by a common inventor(s).

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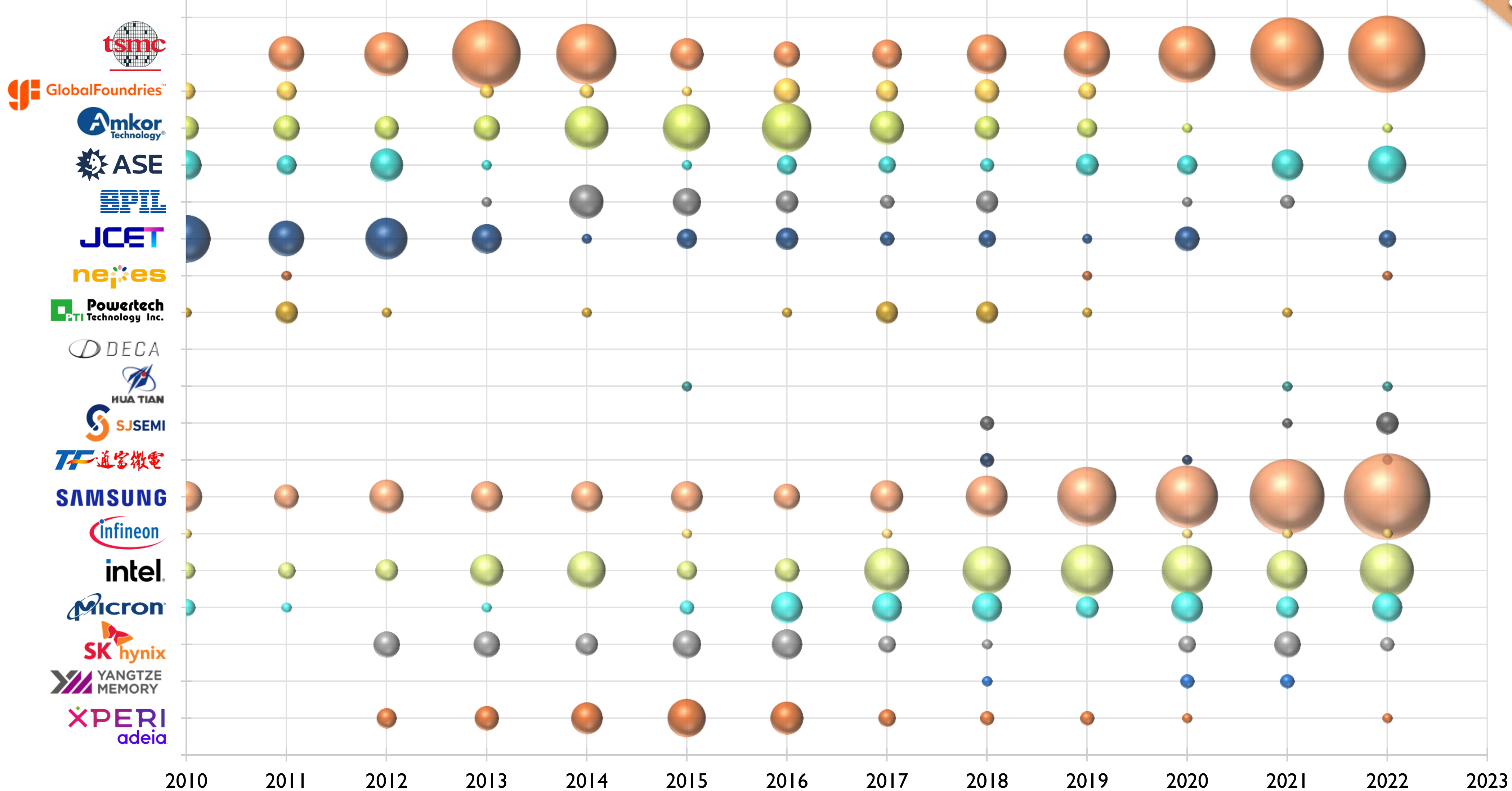
MAIN TRENDS
Silicon interposer



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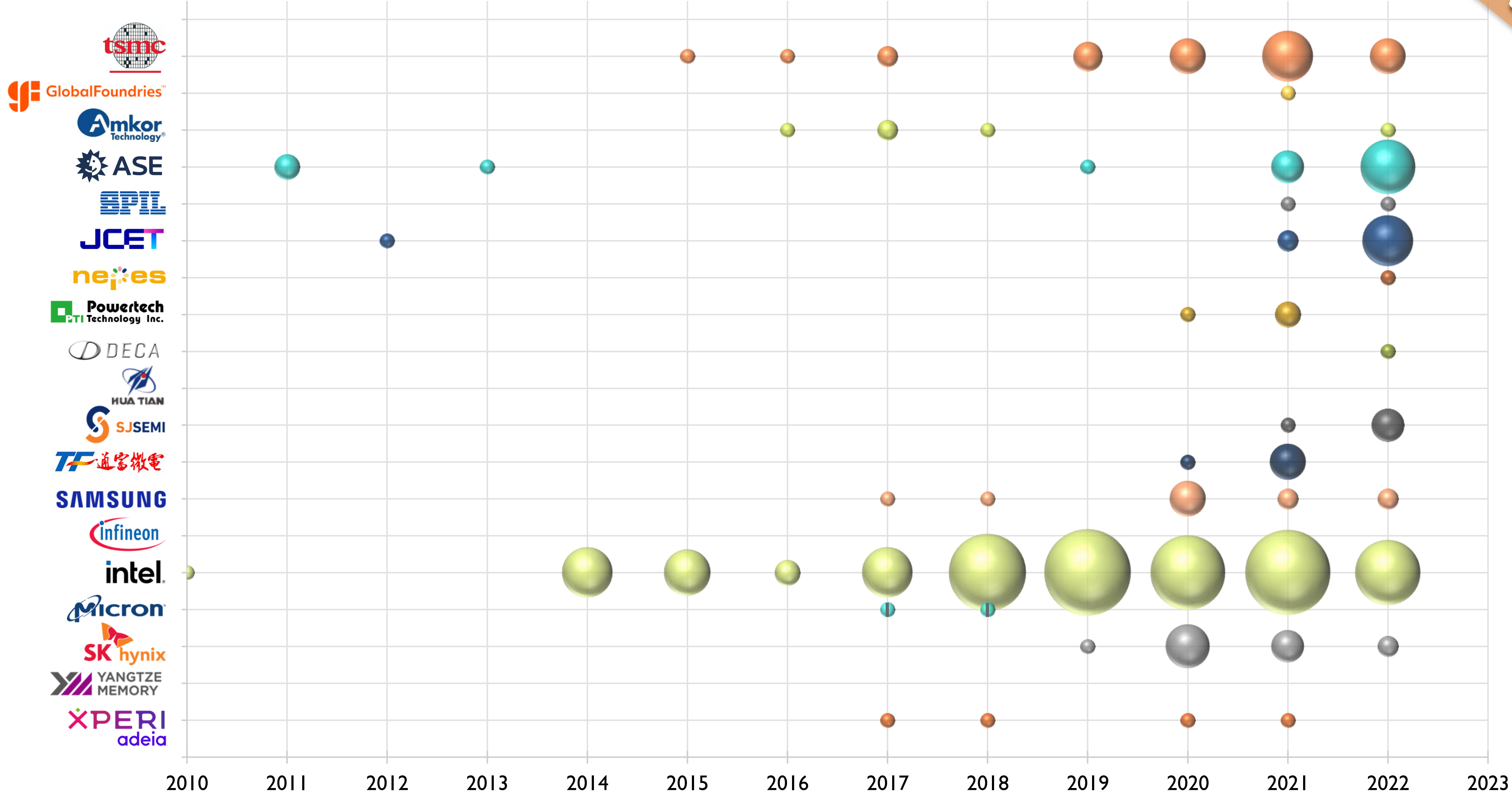
MAIN TRENDS

Embedded interconnect bridge

SAMPLE



Bubble size is related to the number of patent families (inventions). A patent family is a set of patents filed in multiple countries to protect a single invention by a common inventor(s).

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MAIN TRENDS

Hybrid bonding (bumpless direct metal-to-metal and oxide-to-oxide bonding)

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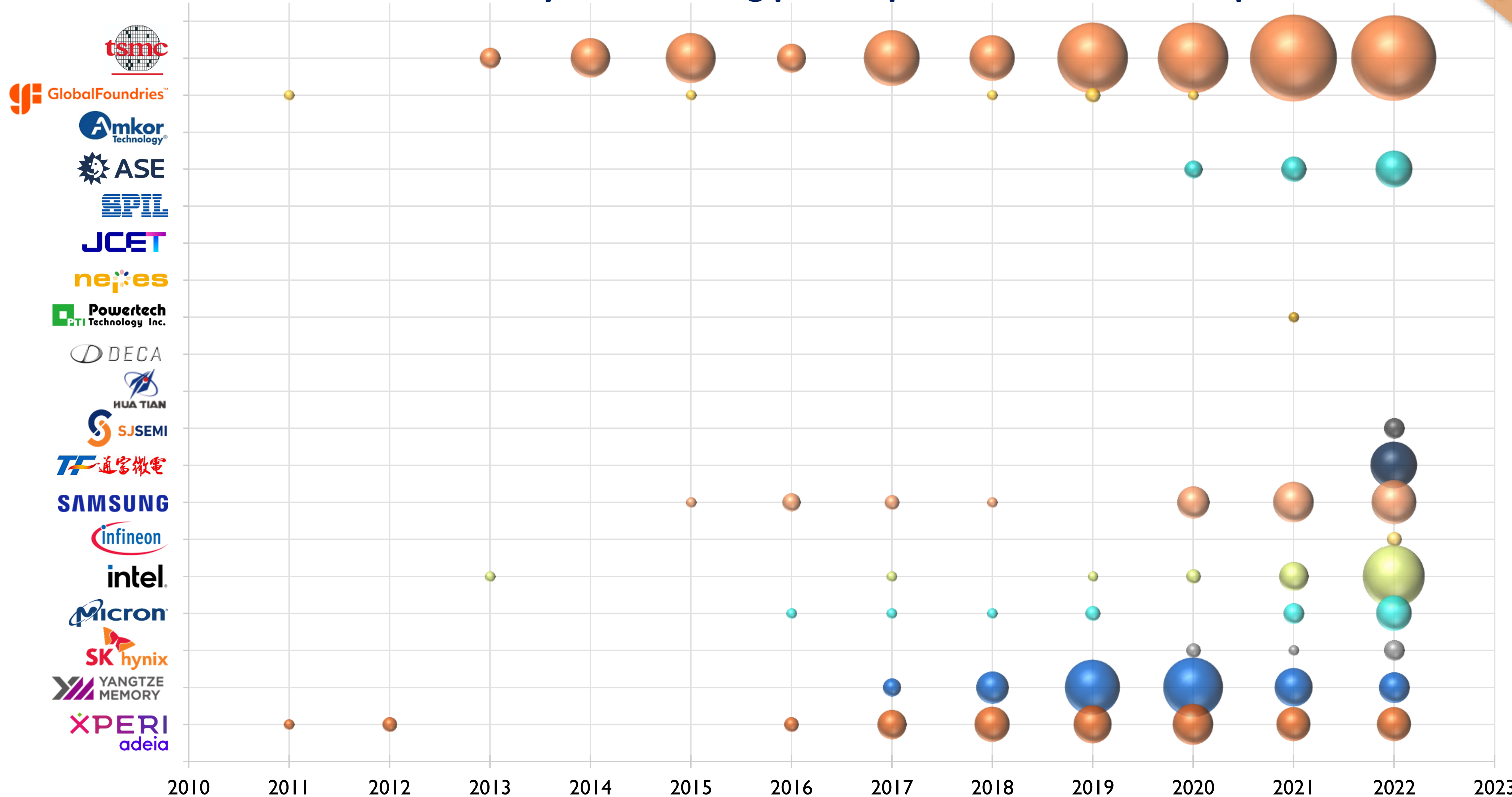
Time evolution of Hybrid Bonding patent publications over the past decade



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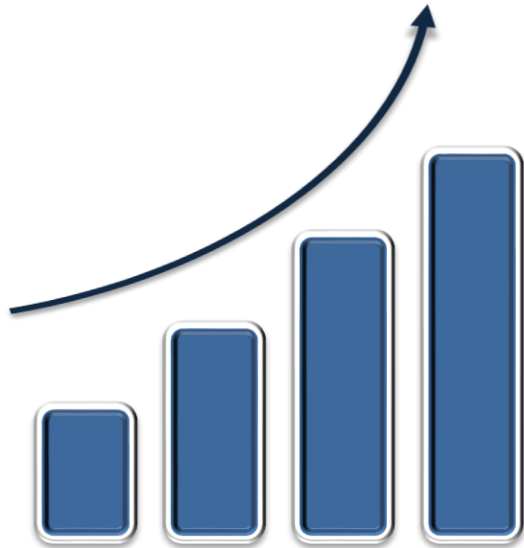

QUARTER OVERVIEW

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Q4 2022 OVERVIEW

Key facts

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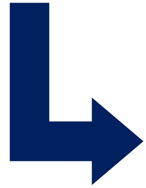

	Q4 2022	Fan Out Packaging		2.5D/3D Integration				Others
		All fan-out packaging (WLP & PLP)	Fan out panel level packaging (FOPLP)	All 2.5D/3D packaging technologies	Interposer / Bridge	Hybrid bonding	3D stacked memory	
New patent families (inventions)	963	101	9	340	276	59	105	564
Patent families newly granted	583	65	3	175	138	36	47	371
Patents expired or abandoned	1008	67	0	68	60	32	3	881
IP collaborations (new co-filings)	5	0	0	1	0	0	1	4
IP transfers (change in ownership)	1	0	0	0	0	0	0	1
US litigations	0	0	0	0	0	0	0	0
EU oppositions	0	0	0	0	0	0	0	0

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Q4 2022 OVERVIEW

Patent families (inventions) newly published and newly granted

*Note: the numbers represent the number of **patent families**. A patent family can belong to multiple segments.*

Patent assignees	Patent families newly published	Patent families newly granted	Fan Out Packaging				2.5D/3D Integration								Others	
			All fan-out packaging (wafer level & panel level)		Fan out panel level packaging (FOPLP)		All 2.5D/3D packaging technologies		Interposer / Bridge		Hybrid bonding		3D stacked memory			
			Newly published	Newly granted	Newly published	Newly granted	Newly published	Newly granted	Newly published	Newly granted	Newly published	Newly granted	Newly published	Newly granted	Newly published	Newly granted
Intel	243	155	1	7			134	71	123	69	19	3	30	18	109	83
Samsung Group	205	128	30	14	8	1	76	27	61	16	6	1	27	11	111	91
TSMC	161	76	15	24		1	81	46	64	34	22	20	36	13	80	21
ASE	64	49	4	6			9	10	9	7		4			52	35
JCET Group	47	10	9	2			4	1	4	1					36	8
Huatian Technology	39	19	10	5			1		1						28	14
Infineon	39	28		2			1		1						38	26
Micron	32	29	2				10	6	1		5	2	4	4	22	23
YMTC	25	6	1				2	1			2	1			22	5
SJSemi	23	10	11				10	3	8	3	2		3		6	7
GlobalFoundries	20	22													20	22
Tongfu Microelectronics (TFME)	18	16	7	1			7				2		5		11	15
SK Hynix	15	10	2				4	2	3	2	1				6	7
SPIL	10	4	4	2			1	2	1	2					6	1
Powertech Technology (PTI)	7	8	1	1			1	1	1	1					6	7
Nepes	5	2	4	1	1	1	1		1						1	1
Amkor Technology	0	2														2
Deca Technologies	0	1						1		1				1		
Xperi/Adeia	0	5						5		3		5				

- **Intel** has been the most active patent applicant with 243 new patent families published this quarter, followed by **Samsung** and **TSMC**. For both, the focus is on Interposer/Bridge technologies. **TSMC** has strengthened its IP position in **FO packaging** and **hybrid bonding** with respectively 24 and 20 inventions newly granted.
- The 2022 Q4 IP activity of OSATs is more focus on 'others' segment, except for **SJSemi** which has been mainly active on **FO** and **Interposer** segments.
- **Micron** and the other memory makers published inventions related to hybrid bonding, which is an important process for memory device stacking.
- The non-practicing entity (NPE) **Xperi** did not publish any new invention this quarter, but it has been granted for new IP rights in **hybrid bonding**.

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Q4 2022 OVERVIEW

Expired and abandoned patents

SAMPLE

*Note: the numbers represent the number of **patents**. A patent can belong to multiple segments.*

Patent assignees	Expired or abandoned patents	Fan Out Packaging		2.5D/3D Integration				Others
		All fan-out packaging (wafer level & panel level)	Fan out panel level packaging (FOPLP)	All 2.5D/3D packaging technologies	Interposer / Bridge	Hybrid bonding	3D stacked memory	
Samsung Group	191	4						187
TSMC	158	23		54	46	32		89
Infineon	126	16		5	5			105
ASE	106							106
GlobalFoundries	77	1						76
Intel	76			4	4		3	72
Micron	73			4	4			69
Amkor Technology	45	20						25
Powertech Technology (PTI)	22	3						19
SPIL	21							21
Xperi/Adeia	16							16
SK Hynix	11							11
JCET Group	8							8
Tongfu Microelectronics (TFME)	8							8
Nepes	2							2
Deca Technologies	1							1
SJSemi	1							1
Huatian Technology								
YMTC								

- This quarter, **TSMC** is the player that has lost the most capacity to hamper the freedom of operate of its competitors in advanced packaging segments **FO**, **Interposer/Bridge** and **Hybrid Bonding**.
- The most important IP protection loss for **Infineon** is FO technology, with 16 patents expired this quarter for 2 new granted patents and no new published inventions.
- **Amkor** has lost 20 patents on **FO** this quarter while no new patent applications have been published in key packaging technologies.

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Q4 2022 OVERVIEW

Main IP collaborations (patent co-filings)

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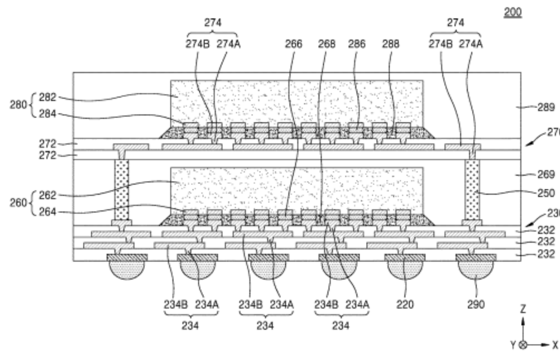
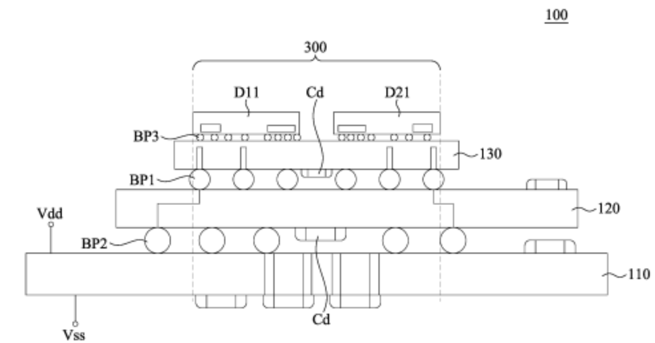
These table shows the main new collaborations on advanced packaging that have led to the co-filing of new patent applications involving at least one player we monitor in this Advanced Packaging Patent Monitor.

Patent co-applicants	Patent applications	Title	Segments
SAMSUNG ELECTRONICS KPX CHEMICAL	US20220350253	Compositions for removing photoresists and methods of manufacturing semiconductor devices and semiconductor packages using the compositions	2.5D/3D packaging
TSMC GLOBAL UNICHIP	US20230144129	Semiconductor chiplet device	2.5D/3D packaging



The inventive concept provides a photoresist-removing composition, which may cleanly remove a photoresist pattern used in a process of manufacturing a unit element, without adversely affecting (e.g., corroding) metal-containing components around the photoresist pattern. According to an aspect of the inventive concept, there is provided a photoresist-removing composition that includes a polar organic solvent, an alkyl ammonium hydroxide, an aliphatic amine not including a hydroxy group, and a monovalent alcohol.



The present disclosure relates to a semiconductor chiplet device, especially a structure in which multiple dies are connected through an interposer layer.
The first die and the second die are configured to perform a data transmission through the first interface, the interposer layer and the second interface. the least one decoupling capacitor is arranged between the the first interface and the second interface, or is arranged in a vertical projection area of the first interface and the second interface on the packaging substrate.

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Q4 2022 OVERVIEW

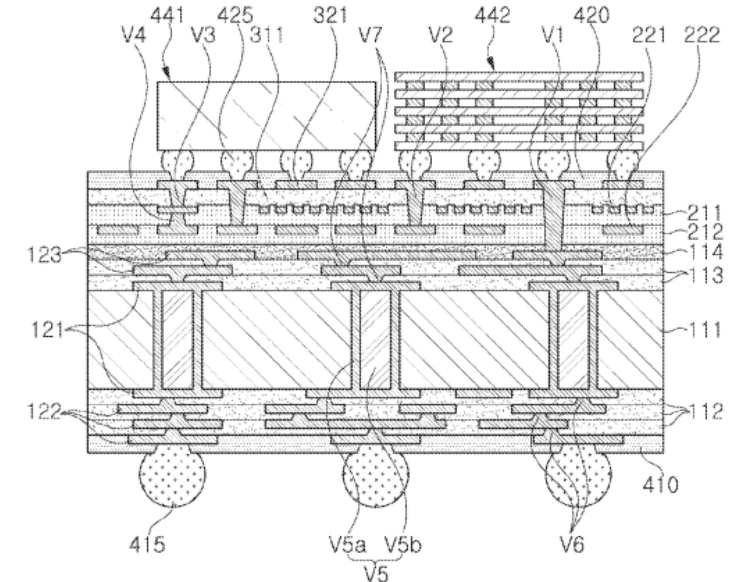
Main IP transfers (change in patent ownership)

SAMPLE

These table shows the main new IP transfers on advanced packaging that have led to the re-assignment of patent from/to at least one player we monitor in this Advanced Packaging Patent Monitor.

IP transfer	Date	Transferred patent	Topic	Segments
From **Samsung Electro-Mechanics** To **Kia Motors** and **Hyundai Motors**	Oct 2022	US11521922	Printed circuit board which may replace a silicon interposer	2.5D/3D packaging

In October 2022, the IP rights of the patent US11521922 owned by **Samsung Electro-Mechanics** were acquired by **Kia** and **Hyundai Motors**. The invention relates to a printed circuit board. The **interposer** market has been growing due to a high specification of a set and employment of a high bandwidth memory (HBM). Mostly, silicon has been used as a material for an **interposer**. For example, in the case of a semiconductor package using an **interposer**, a die may be surface-mounted on a **silicon interposer** and molded with a molding material. Due to the increase in the number of HBMs, an **interposer** has also been designed to have high performance, and accordingly, the difficulty of process may increase, and the issue of a lowered yield has emerged. An aspect of the present disclosure is to provide a printed circuit board which may easily implement a microcircuit pattern. Another aspect of the present disclosure is to provide a printed circuit board which may secure sufficient adhesive force between a microcircuit pattern and an insulating material. Another aspect of the present disclosure is to provide a **printed circuit board which may replace a silicon interposer**.



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Litigations

US IP litigations open/closed during the quarter

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No US IP litigation related to advanced packaging have been filed or closed in the quarter

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Oppositions

Oppositions to European patents

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No new oppositions have been filed at the EPO against packaging-related European patents

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PLAYERS IP ACTIVITY DURING THE QUARTER

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Pure Play Foundries

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TSMC

Q4-2022 IP ACTIVITY

Note: A patent family/patent can belong to multiple segments.

	Q4 2022	SEGMENTS						
		All Fan-Out packaging	FO - Panel level	All 2.5D/3D packaging	Interposer / Bridge	Hybrid bonding	3D-stacked memory	Others
New patent families (inventions)	**161**	**15**		**81**	**64**	**22**	**36**	**80**
Patent families newly granted	**76**	**24**	**1**	**46**	**34**	**20**	**13**	**21**
Patents expired or abandoned	**158**	**23**		**54**	**46**	**32**		**89**

SAMPLE

- In Q4-2022, the IP activity of **TSMC** is addressing all segments in the scope of this monitor, except for the very specific FO-Panel level segment.

- In FO packaging segment, this quarter TSMC's new patent application addressed **thermal management**, **warpage and stress control**, **and reliability**.
  - **Warpage/stress control:** Structural engineering is favored by **TSMC**. In the new patent application US20230066370, a conductive pattern with an **ellipse-like shape** and a conductive via **shifted outward** result in **stress reduction**. In the US20220352060, a **stacked via structure** is capable of **minimize the via the crack issue** resulted from **concentrated stress**. The introduction of dummy dies (new granted patent US11515268), wall structure (new patent application US20220406729), and a ring-shaped dummy die (new patent application US20220367383) is also key to control structural stress. Material choice is also important. In the new granted patent US11482497, the CTE difference between the encapsulant and the encapsulant layer is chosen to be less than the CTE difference between the encapsulant and the semiconductor substrate of the die.
  - **Heat management:** In the new granted Taiwanese patent TWI788025, **TSMC** claim InFO packages including **thermal dissipation blocks** (pending US patent application US20230037331).
  - **Electrical reliability:** In the new patent application US20230067826, via structures are made of conductive material with lower hardness. The redistribution layer structure is easier to land over the via structure, and the via structure profile may be well-controlled. **The bridge defects may be reduced, and the electrical failure may be prevented.**

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TSMC

Q4-2022 IP ACTIVITY

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- **TSMC** was the most active in the 2.5D/3D, especially for Interposer/Bridge.
  - **Heat management:** An interposer containing line-shaped interposer is disclosed in the new patent application US20220406723. The line-shaped via may provide a greater contact surface area between first metal trace and second metal trace. Heat is more effectively transferred through a greater contact area, the line-shaped via improves power integrity and thermal performance.
  - **Warpage:** A **warpage release layer structure** is formed over the interposer substrate and includes at least one organic material layer in direct contact with the upper surface of the semiconductor die and a high CTE material layer formed over the organic interposer (new patent application US20230010707). Another possibility to control warpage is the use of an interposer with warpage-relief trenches in non-routing regions of the interposer (US20220344280). The method also includes depositing a warpage-relief material in the warpage-reducing trenches. The structure of the interposer can be modified in order to manage stress. In the new granted patent TWI787076, **TSMC** claims a method for forming an interposer with redistribution layer structures in adjacent via layers extending in different directions (see also the pending US patent application US20220336359). The via structure connecting the traces of the redistribution layer structures are therefore in different cross-sectional views. Therefore, the effect of CTE mismatch between the device and the substrate may be reduced, and the strain the via structure suffered may be further reduced.
  - **Speed:** In new granted patents US11482497 and US11462495, **TSMC** claim a **bridge die** for connecting devices dies, which may provide high speed channel between the device dies. Placing a serializer/de-serializer die proximate to a sidewall of a substrate allows a length of electrical pathways to be reduced, thus **reducing impedance and RC delay**. The use of **smaller, separate, interposers** also **reduces complexity of fabrication of interposers and similarly lowers impedance** associated with redistribution interconnect structures and the interposers (see the new patent application US20220415867).
  - **Process:** Organic interposer dicing process is improved to avoid delamination (new patent application US20230023268).
  - **Hybrid Bonding:** The hybrid bonding technique is used by **TSMC** for connecting electronic devices to redistribution structures (RDLs) as disclosed in the new patent applications US20230012157 and US20220381985, and semiconductor die to the dielectric layer of a thermal dissipation structure (see the US20230068578). **TSMC** is also improving the wafer-wafer bonding via wafer bonding systems and plasma activation (US20230010038, US20230067346).

- **TSMC** shown IP activity this quarter on 3D-stacked memories. In the new patent application US20220415867, High-Bandwidth Memory dies (HBM) are integrated with a SoC die. **To minimize ohmic losses and RC delay, the SoC die and the HBM die may be disposed on an interposer**. **Reliability** of packaged memory dies is improved in the pending patent application US20230035212, where a memory device including a base semiconductor die, conductive terminals, memory dies, an insulating encapsulation and a buffer cap is provided. Buffer caps improve the reliability of the package.

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GlobalFoundries

Q4-2022 IP ACTIVITY

GlobalFoundries™

SAMPLE

Note: A patent family/patent can belong to multiple segments.

	Q4 2022	SEGMENTS						
		All Fan-Out packaging	FO - Panel level	All 2.5D/3D packaging	Interposer / Bridge	Hybrid bonding	3D-stacked memory	Others
New patent families (inventions)	**20**							**20**
Patent families newly granted	**22**							**22**
Patents expired or abandoned	**77**							**76**

- This quarter, there is no noticeable inventions newly published or granted on key advanced packaging technologies. Among the newly published patent families, inventions are more focused on **electro-optics** for which packaging possibilities are described. Other patents focus **on ICs, interconnects, logic and memory**, where packaging possibilities are proposed.
- **GlobalFoundries** lost IP protection shares in Q4-2022 with 77 newly dead patents. These patents belong to the category "others". We do not describe them, but they are available in the Excel file.

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OSAT

(outsourced semiconductor assembly and test companies)

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Amkor Technology

Q4-2022 IP ACTIVITY

Note: A patent family/patent can belong to multiple segments.

	Q4 2022	SEGMENTS						
		All Fan-Out packaging	FO - Panel level	All 2.5D/3D packaging	Interposer / Bridge	Hybrid bonding	3D-stacked memory	Others
New patent families (inventions)								
Patent families newly granted	**2**							**2**
Patents expired or abandoned	**45**	**20**						**25**

- In Q4-2022, **Amkor** lost invention protection shares in **Fan-Out packaging** due to the expiration of about 20 US patents belonging to 2 patent families (first published patents US6905914 and US6841874). These two inventions are related to wafer level package, and some members mention Fan-Out traces. These inventions have been carefully kept alive by Amkor over the past 20 years, which shows the importance of these patents to the company. The critical patent family US6905914 (18 US members) discloses a **wafer level package** and fabrication method with **bond pads that are electrically connected to the corresponding first vias without the use of a solder**, e.g., without the use of flip chip bumps, and without the need to form a solder wetting layer, e.g., a nickel/gold layer, on the bond pads. This **maximizes the reliability of the electrical connection** between the first vias and the bond pads, while at the same time **minimizes impedance**.

- Another critical patent family belonging to the segment "Others" (US6930256 and 8 other US members) discloses a semiconductor package having **laser-embedded terminals** in order to provide a **high-density and low cost internal/external mounting and interconnect structure** for integrated circuits.

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ASE

Q4-2022 IP ACTIVITY

ASE

Note: A patent family/patent can belong to multiple segments.

	Q4 2022	SEGMENTS						
		All Fan-Out packaging	FO - Panel level	All 2.5D/3D packaging	Interposer / Bridge	Hybrid bonding	3D-stacked memory	Others
New patent families (inventions)	64	4		9	9			52
Patent families newly granted	49	6		10	7	4		35
Patents expired or abandoned	106							106

- This quarter, **ASE** had IP activity related to Interposer/Bridge, and more specifically **bridge dies** (new published invention US20220415851, and patent families firstly granted US11508655, US11462484).

- **ASE** got 4 newly granted invention in the field of **hybrid bonding**. Issues related to **bond strength** are addressed in the new granted patent US11538756. The bonding structure includes a NT-Cu layer having anisotropic crystal structure, which allows for a **more uniform thermal expansion** at a top surface of the NT-Cu layer. **Superior bonding strength and electrical connection** between two bonded NT-Cu layers is achieved. **Alignment of connections** between semiconductor structures in contact is addressed in the new granted patent US11538778, where a semiconductor package includes an alignment material (an organic dielectric material and a notch). In the US11495557 a method allows to **decrease the bonding temperature process**, in order to limit damages on the semiconductor materials when using standard hybrid bonding process. A surface treatment is provided. In the US11502024, **ASE** claims **redistribution layers on two sides** of a semiconductor element to provide electrical connections with **faster transmission speed and smaller package**. The semiconductor active surface and the **RDL are connected by hybrid bonding**.

- Regarding the Fan-Out packaging segment, **reliability improvement of the FO process** is claimed in the new granted patent US11515249. The risks of the narrow-in-line/space fan-out structure peel-off can be significantly reduced by **embedding a portion of the conductive layer** in the dielectric layer. Finally, in the new patent family US20220384308 published this quarter, an improved FO package is disclosed for structures that include a decoupling capacitor, such as a deep trench capacitor (DTC) die, and an integrated circuit (IC) die. The package allows the DTC die to be electrically connected to the IC die by a **shorter electrical path**.

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SPIL

Q4-2022 IP ACTIVITY

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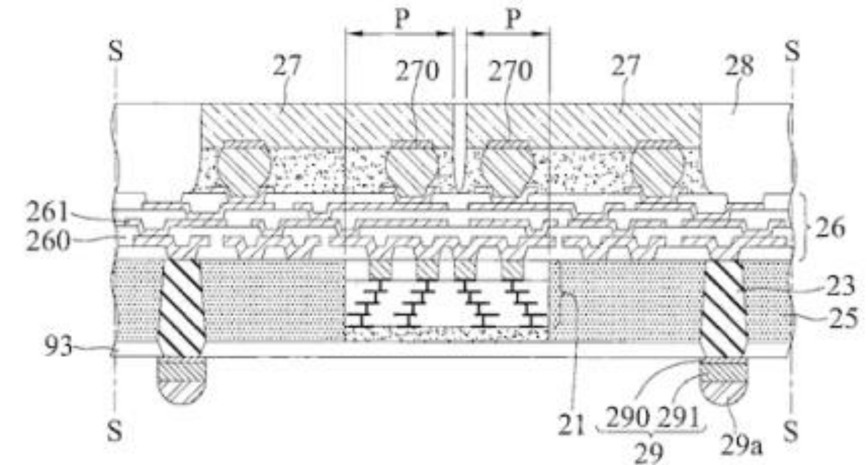
Note: A patent family/patent can belong to multiple segments.

	Q4 2022	SEGMENTS						
		All Fan-Out packaging	FO - Panel level	All 2.5D/3D packaging	Interposer / Bridge	Hybrid bonding	3D-stacked memory	Others
New patent families (inventions)	**10**	**4**		**1**	**1**			**6**
Patent families newly granted	**4**	**2**		**2**	**2**			**1**
Patents expired or abandoned	**21**							**21**

- **Fan-Out packaging** has been the most active segment for **SPIL** this quarter, with structural improvements of the package. In the new granted patent TWI788230, a local high wiring configuration (member 21) in combination with a local low wiring (carrier structure 26) wiring design (member 21 replaces a portion of the RDL form line layer 261 of the carrier structure 26). The carrier structure 26 not only maintains a **high L/S line specifications** (e. g., 10/10 microns L/s), but also reduces the number of layers of the connection layers 261 (e. g., less than five layers of line layers 261) to increase the process yield of the carrier structure 26 (or RDL). Thereby **effectively reducing overall process difficulty and reducing manufacturing costs.**



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JCET Group

Q4-2022 IP ACTIVITY

JCET

SAMPLE

Note: A patent family/patent can belong to multiple segments.

	Q4 2022	SEGMENTS						
		All Fan-Out packaging	FO - Panel level	All 2.5D/3D packaging	Interposer / Bridge	Hybrid bonding	3D-stacked memory	Others
New patent families (inventions)	47	9		4	4			36
Patent families newly granted	10	2		1	1			8
Patents expired or abandoned	8							8

- In Q4-2022, JCET showed IP activity on Fan-Out packaging with 9 new patent families. The new published patent application US20230005811 tackles one of the **important challenges in FO manufacturing, namely warpage/bending and thermal stress management**. By providing a dummy wafer on the redistribution layer and configuring the **dummy wafer to connect to the metal wiring layer**, the dummy wafer can not only function to support the structure and **suppress the warpage**, but also form a continuous **heat dissipation channel,** thereby improving thermal management capability of the fan-out package structure. In the new patent application US20220399254, a **fan-out package structure is formed on the metal lead frame, which improves the heat dissipation** capacity of the chip. Indeed, a fan-out package allows multiple layers of high-density wiring, but is low in reliability and poor in heat dissipation capacity. Lead-frame type packages (such as QFN and QFP, etc.) for chips have the characteristics of low cost, ease of thermal management and high reliability, but can hardly support higher-density wiring, in particular multi-layer wiring. Therefore, in this new patent application **JCET** proposes to combine fan-out and lead-frame packages.

- This quarter, the IP activity of **JCET** on 2.5D/3D packaging relates to a double-sided SiP packaging structure (CN115332195), a package including a silicon interposer and a bridge chip with a reduced thermal stress caused by the mismatch of the thermal expansion coefficients of different package materials (CN217691134), and a silicon-based electronic IC packaging module including a a bridging chip and a Photonic Integrated Circuit (PIC) chip (CN115172185).

- Packaging materials are engineered in new patent application US20220406675. Semiconductor devices are susceptible to heat from operation of the semiconductor die. To **avoid delamination** of the thermal interface material (TIM) and heatsink material, the inventors proposes a **hybrid TIM structure**. The first TIM provides adhesion for joint reliability and the second TIM provides stress relief. Alternatively, a heat spreader is disposed over the first TIM and second TIM and a heat sink is disposed over a third TIM and fourth TIM on the heat spreader.

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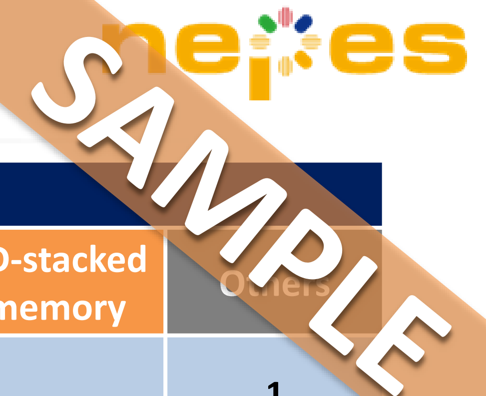
NEPES

Q4-2022 IP ACTIVITY

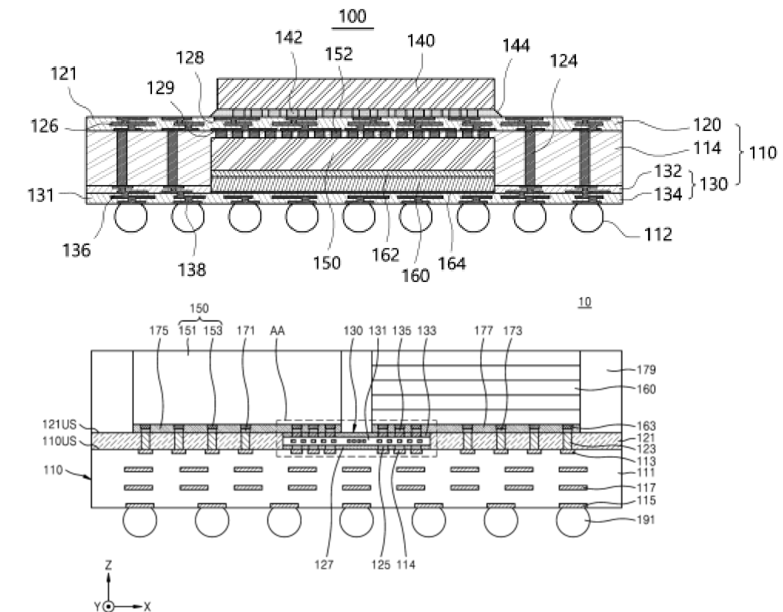


Note: A patent family/patent can belong to multiple segments.

	Q4 2022	SEGMENTS						
		All Fan-Out packaging	FO - Panel level	All 2.5D/3D packaging	Interposer / Bridge	Hybrid bonding	3D-stacked memory	Others
New patent families (inventions)	5	4	1	1	1			1
Patent families newly granted	2	1	1					1
Patents expired or abandoned	2							2

In Q4-2022, **NEPES** has been active on the **Fan-out packaging segment**. It provides a semiconductor package having a structure capable of **improving stress distribution** between the semiconductor FO package and the board (new patent application US20220352059, new granted patent US11476211). **Thermal management** in the package is addressed in the new patent application KR10-2022-0157916. **A heat dissipation layer 160 may be arranged on a lower surface of the internal chip 150**. The heat dissipation layer 160 may be formed of copper or aluminum material having excellent thermal conductivity or an alloy of a mixture of a plurality of materials.

In the new patent application KR10-2022-0145782, the first semiconductor chip and the second semiconductor chip are electrically connected to each other through a relatively **short electrical connection path through the bridge chip and / or the redistribution structure**, thereby providing a semiconductor package having **improved electrical characteristics such as power integrity and signal integrity.**



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Powertech Technology (PTI)

Q4-2022 IP ACTIVITY

Powertech Technology Inc.

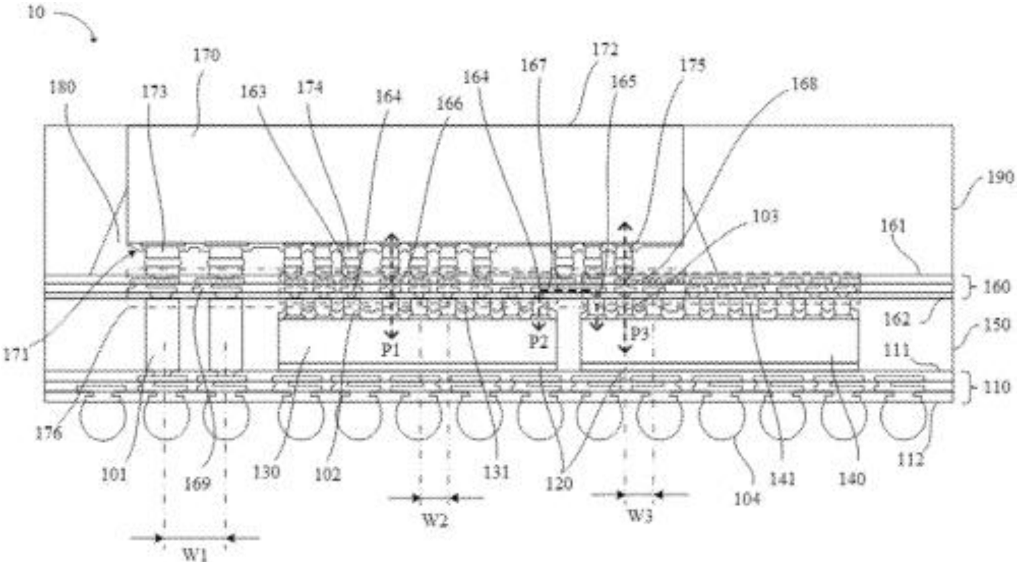
SAMPLE

Note: A patent family/patent can belong to multiple segments.

	Q4 2022	SEGMENTS						
		All Fan-Out packaging	FO - Panel level	All 2.5D/3D packaging	Interposer / Bridge	Hybrid bonding	3D-stacked memory	Others
New patent families (inventions)	7	1		1	1			6
Patent families newly granted	8	1		1	1			7
Patents expired or abandoned	22	3						19

- In Q4-2022, **PTI** has been granted of a new Taiwanese patent TWI788045 in which a **passive element (130) is integrated to a multi-chip FO package** to make an electrical **connection between multiple components without increasing a package size.**

- PTI has lost the patent TWI646640 (fees not paid) related to a FO structure with a heatsink. The patent family comprises still alive patent US10224254 and CN108807308.



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Deca Technologies

Q4-2022 IP ACTIVITY

DECA

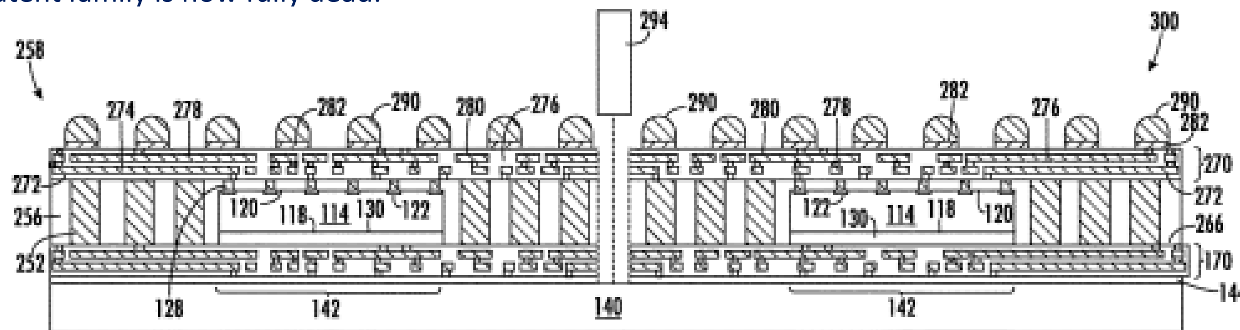
SAMPLE

Note: A patent family/patent can belong to multiple segments.

	Q4 2022	SEGMENTS						
		All Fan-Out packaging	FO - Panel level	All 2.5D/3D packaging	Interposer / Bridge	Hybrid bonding	3D-stacked memory	Others
New patent families (inventions)								
Patent families newly granted	1			1	1		1	
Patents expired or abandoned	1							1

- In Q4-2022, **Deca** got a new patent granted in the US (US11538759) related to a fully **molded bridge interposer** (the patent family comprises also Korean, Chinese and Taiwanese pending patent applications). In this US granted patent, **the increased electrical connection density is provided with a fully molded bridge interposer**, consisting of a bridge die, copper posts, and an encapsulant. The interposer may be used to connect **high bandwidth memory (HBM)** to a semiconductor structure.

- The lost patent US6730532 is the last of an 8 US patent family regarding a m method and system for universal packaging in conjunction with an automated in-line back-end IC manufacturing process. This patent family is now fully dead.



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Huatian Technology

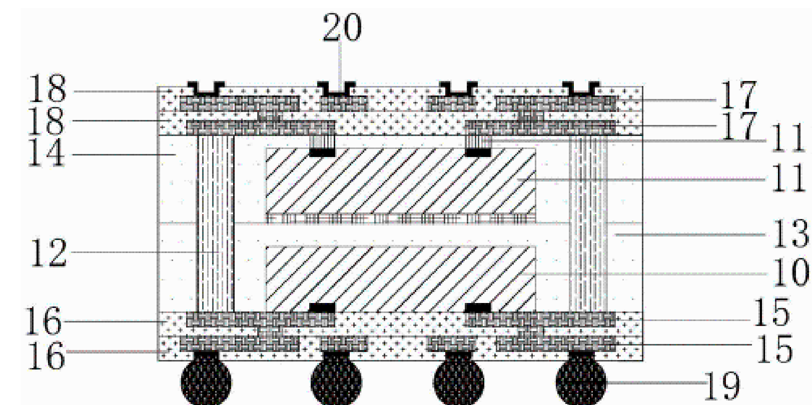
Q4-2022 IP ACTIVITY

SAMPLE

Note: A patent family/patent can belong to multiple segments.

	Q4 2022	SEGMENTS						
		All Fan-Out packaging	FO - Panel level	All 2.5D/3D packaging	Interposer / Bridge	Hybrid bonding	3D-stacked memory	Others
New patent families (inventions)	39	10		1	1			28
Patent families newly granted	19	5						14
Patents expired or abandoned								

- This quarter, the new patent families published by **Huatian** are directed towards **three-dimensional integrated FO packaging** structure. The **packaging volume is reduced** while satisfying the performance of the chip, interconnection is made in the Z direction, and signal loss is reduced while reducing cost (CN218069843, CN218069834, CN115472583, CN217955850, CN115295529, CN217562552, CN115188677).
- A new invention relates to an **interposer** structure (CN115360188). It discloses a packaging method using **TSV chips** and an **interposer substrate**, which allows **chips with different sizes to be stacked together** and at the same time improves space utilization on one substrate.
- There were no expired or abandoned patents in Q4-2022.



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SJSEMI

Q4-2022 IP ACTIVITY

SJSEMI

Note: A patent family/patent can belong to multiple segments.

	Q4 2022	SEGMENTS						
		All Fan-Out packaging	FO - Panel level	All 2.5D/3D packaging	Interposer / Bridge	Hybrid bonding	3D-stacked memory	Others
New patent families (inventions)	**23**	**11**		**10**	**8**	**2**	**3**	**6**
Patent families newly granted	**10**			**3**	**3**			**7**
Patents expired or abandoned	**1**							**1**

- **SJSemi** published new inventions on Fan-Out packaging technology to package a wide variety of devices, while also working on Fan-Out packaging improvement. The new patent application CN115458417 discloses a FO package which integrates a bridge to improve the density of the I/O in. Regarding antennas, a FO packaging structure radiating electromagnetic wave in horizontal direction and vertical direction with the advantage of reduced package thickness is disclosed in the new patent application US20220320748 and US20220319870. Besides, more and more wafer level packages need to integrate RF integrated passive device (RF IPD), such as a filter. In the new published invention CN115346965, **SJSemi** proposes to integrate a 3D IPD into the wafer level package by preparing the integrated 3D IPD structure inside the molding layer.

- This quarter, **SJSemi** published new invention in which **hybrid bonding** is used in the FO process. For instance, in the new patent application CN115360102 the first rewiring layer and the semiconductor chip are bonded without solder by using the hybrid bonding structure, so **that cracks of solder on the interface of the first rewiring layer and the semiconductor chip are avoided**, the interconnection **reliability is improved**. **Hybrid bonding** is also integrated in the FO package for **higher I/O density** as disclosed in the CN115206948.

- Regarding the 3D stacked memory segment, in the CN115332169 , the bonding of **HBM wafers is made by including a bonding element at the edge of the wafer**, rather than by using hybrid bonding. The goal is to overcome hybrid bonding limitation (contact flatness and cost).

SAMPLE

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Tongfu Microelectronics

Q4-2022 IP ACTIVITY

SAMPLE

Note: A patent family/patent can belong to multiple segments.

	Q4 2022	SEGMENTS						
		All Fan-Out packaging	FO - Panel level	All 2.5D/3D packaging	Interposer / Bridge	Hybrid bonding	3D-stacked memory	Others
New patent families (inventions)	18	7		7		2	5	11
Patent families newly granted	16	1						15
Patents expired or abandoned	8							8

- This quarter, **Tongfu** IP activity is focused on FO process improvement. It got a new granted patent CN111312598 in which a package processing can be achieved on the whole wafer without carrying out a chip pasting process. In new published inventions CN115411027 and CN115394661, the implementation of **grooves improves the FO process**. The main chip is arranged in the groove on the substrate, so that the fan-out type packaging device has smaller overall volume. In another new patent application CN115312398, **several grooves** are used. **The first main chip and the second main chip are arranged in the first groove and the second groove**, so that the overall **height of the packaged device is reduced**, the first conductive hole can be formed in the substrate, so that the **signal or data interaction between other elements and the substrate is facilitated**, and the overall **performance of the packaged device is improved**. In addition, **the substrate has higher rigidity**, and is beneficial to **reducing the probability of warping** in the packaging process.

- Similarly, to SJSemi, **hybrid bonding is integrated to FO processing** in order to shorten the distance between the interconnections of the packaging structure, reduce the thickness of the packaging, increase the I/O density of chip packaging, and reduce the electric signal impedance and the packaging thermal resistance (see new patent application CN115527869).

- Regarding 3D-stacked memory, **Tongfu** is integrating HBM among the dies process via the FO process.

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SAMPLE

IDM

(integrated device makers)

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SAMSUNG

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Note: A patent family/patent can belong to multiple segments.

	Q4 2022	SEGMENTS						
		All Fan-Out packaging	FO - Panel level	All 2.5D/3D packaging	Interposer / Bridge	Hybrid bonding	3D-stacked memory	Others
New patent families (inventions)	205	30	8	76	61	6	27	111
Patent families newly granted	128	14	1	27	16	1	11	91
Patents expired or abandoned	191	4						187

Samsung foundry service developed the I-Cube™ & H-Cube™ 2.5D package and the 3D IC X-Cube™ package for heterogenous integration. In Q4-2022, **Samsung is still positioned as a strong IP leader on 2.5D/3D packaging technologies**.

- **Improved interposer fabrication.** Fabrication costs are cut down by simplifying the fabrication process in the new granted patent US11482483. In the new published patent application US20220352110, **the adhesion reliability** between interposer and chips is improved by fabricating an **interposer substrate including a cavity**, where the semiconductor chip is positioned. **An adhesive layer is positioned inside and outside the cavity**, wherein the adhesive layer is formed on all of the upper and side surfaces of the semiconductor chip, or on the side surfaces of the semiconductor chip. Regarding the process step of **interposer detachment**, the patent US11521863 newly granted this quarter claims **a release film including a light absorber and a gas foaming agent** that may be used to **prevent residues of the release film from being left on the interposer substrate**. **Samsung** is also **functionalizing the interposer**. A capacitor can be inserted in the interposer, with a simplified process as claimed in the new granted patent US11538747. Besides, the **electrical path** between chips and capacitor is shortened as described in the new patent application US20220384351.
- **Warpage.** In the new granted patent US11502061, the warpage control is facilitated with an **interposer partitioned into a plurality of regions through a groove** and having a plurality of semiconductor chips, and a mold, filling the space between the plurality of chips. Another possibility proposed by Samsung to avoid warpage is to **include a capping structure** on the interposer substrate as disclosed in the new patent application US20220392844. The **width or length of an interposer substrate may be reduced to decrease the stress** applied to the interposer substrate and causing the molding layer to delaminate (see the inventions disclosed in the US20220328445.
- **Mold reliability.** The molding material used around the different semiconductor parts positioned on the interposer may be cured before completely filling a gap, resulting in voids. In the new patent application US20220359466, **Samsung** uses a pad-free region reserved on the interposer, that serves as an **injection passage of the molding material**. The interposer package is optimized to assemble a **3D complex structure** including an upper semiconductor **chip and a chip stack** as disclosed in the patent application US20220352138.

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Samsung Group

Q4-2022 IP ACTIVITY

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Samsung Fan-Out related patent activity is different from other IP players due to the importance of **panel level packaging** IP. FO panel level packaging is one-third of Samsung FO new patent families published in Q4-2022. For instance, in the new patent application US20220415802, the semiconductor package may be manufactured at panel level.

- According to its Q4-2022 IP activity, **Samsung** is improving the FO process reliability in terms of **packaging efficiency, electric interferences and warpage.** In the new patent application US20220399260, a fan-out semiconductor package is configured to **increase a distance between I/O terminals**, in order to **alleviate the interference** between the I/O terminals. In the US20220336336, a **fan-out panel level package** accommodates **chips of various sizes.** The US20220415771 discloses a semiconductor package that may include a protection pattern covering the top and side surfaces of the under-bump pattern. This will reduce or **prevent delamination or crack** at the interface between the under-bump pattern and the protection pattern. In the new patent application US20220406697, **a redistribution layer alleviates the stress caused by the coefficient of thermal expansion difference** between a semiconductor chip and the stack via structure.

- FO packaging improvements also address antennas this quarter. In the new patent application US20220415802, the active surface of the semiconductor chip may be disposed in a direction toward the **antenna substrate**. Thus, an electrical path may be shortened, thereby **improving signal transmission speed, the thickness of the semiconductor package may be reduced** as compared to a case in which internal connection lines are disposed in an antenna substrate. Further, **pattern delamination and/or short** caused when internal connection lines are formed in an antenna substrate may be **mitigated or prevented**, thereby improving the **electrical reliability** of the semiconductor package. The molding layer may be in contact with the active surface and the inactive surface of the semiconductor chip. Thus, the **warpage phenomenon of the semiconductor package may be effectively controlled.**

- This quarter **Samsung** showed also IP activity related to 3D-stacked memories. Those inventions includes memory chips, HBM, among the chips that are packaged.

- Finally, a theme that is important for **Samsung**, due to stacking dies to achieve a high capacity, is **thermal management**. To improve performance in such a case, the new patent application US20220359341 discloses a thermoelectric **cooling layer** integrated to the package.

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Infineon

Q4-2022 IP ACTIVITY

Note: A patent family/patent can belong to multiple segments.

	Q4 2022	SEGMENTS						
		All Fan-Out packaging	FO - Panel level	All 2.5D/3D packaging	Interposer / Bridge	Hybrid bonding	3D-stacked memory	Others
New patent families (inventions)	39							38
Patent families newly granted	28	2						26
Patents expired or abandoned	126	16		5	5			105

- **Infineon** has been newly granted for 2 inventions on **Fan-Out packaging**. In the granted DE102020216456 (still pending in US US20220199481 and China CN114725038), a chip arrangement in the form of an **embedded Wafer Level Ball Grid Array (eWLB)** is designed to dissipate heat from the semiconductor chip. The new granted DE102020132641 (still pending in US US20220181246 and China CN114628345) claims an electrical **redistribution layer** configured to carry an electrical signal having a wavelength.
- **Infineon** lost several patents related to **FO packaging** and belonging to 5 patent families. One of patent families is now fully dead (US8659154, US9984900, DE102009011975). This seminal patent families (priority date: 2008) relates a solution to avoid the small passive components to slip and break contact with the carrier foil during the molding process when active and passive components are combined into a single module using eWLB technology.

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Intel

Q4-2022 IP ACTIVITY

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Note: A patent family/patent can belong to multiple segments.

	Q4 2022	SEGMENTS						
		All Fan-Out packaging	FO - Panel level	All 2.5D/3D packaging	Interposer / Bridge	Hybrid bonding	3D-stacked memory	Others
New patent families (inventions)	**243**	**1**		**134**	**123**	**19**	**30**	**109**
Patent families newly granted	**155**	**7**		**71**	**69**	**3**	**18**	**83**
Patents expired or abandoned	**76**			**4**	**4**		**3**	**72**

- In Q4-2022, the IP activity of **Intel** is addressing all the main segments in the scope of this monitor. The IP activity is strong to protect 2.5D & 3D packaging inventions.

- The 2.5D interposer technology is broadly patented by **Intel**. The new patent application US20220406751 discloses a monolithic integration of semiconductor dies, including an **active interposer** (**active device layer**). The active device interposer may be manufactured by **hybrid bonding** as described in the new patent application US20220399324. The pending patent application US20220399294 proposes to combine the **interposer technology with hybrid bonding** in order to **stack dies having different pitches**. **Organic interposers** are less expensive to manufacture than semiconductor- or glass-based interposers and may have electrical performance advantages due to the low dielectric constants of organic insulating materials. In the pending patent applications US20220399305 and US20220399294, **Intel** leverages the advantages of **organic interposers** and the **ultra-fine pitch** achievable by **hybrid bonding** (and previously only achievable when using semiconductor-based interposers). Also interesting, the new patent application US20220399277 discloses selective routing through **intra-connect bridge dies** (intra-connect "jump over" bridge dies or "jump over die"). **Intel** is also putting efforts in protecting **glass substrates as shown by new patent applications published in Q4-2022**: US20220399324, US20220399305, US20220399294, US20220399277, US20220375844, US20220406721.

- The dynamic IP activity of **Intel** is also related to 3D-stacked memories. The inventions pertain to **memory elements, as dies integrated inside a single package** with other dies (computing …). **Intel** is indeed capable of manufacturing complex advanced package as described in the new patent application US20220406721.

- No noticeable IP collaborations. **Intel** appears to be a strong independent IP player in the field of advanced packaging.

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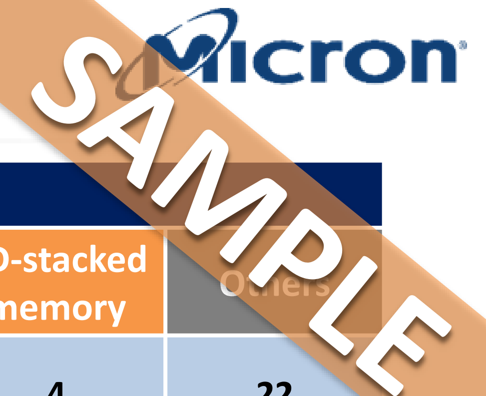
Micron

Q4-2022 IP ACTIVITY



Note: A patent family/patent can belong to multiple segments.

	Q4 2022	SEGMENTS						
		All Fan-Out packaging	FO - Panel level	All 2.5D/3D packaging	Interposer / Bridge	Hybrid bonding	3D-stacked memory	Others
New patent families (inventions)	**32**	**2**		**10**	**1**	**5**	**4**	**22**
Patent families newly granted	**29**			**6**		**2**	**4**	**23**
Patents expired or abandoned	**73**			**4**	**4**			**69**

In Q4-2022, the IP activity of **Miron** is driven by 3D-stacked memories and hybrid bonding.

- In conventional **hybrid bonding** operations can be difficult to align, and moreover can fail when insufficient surface area is available to form mechanically robust oxide-oxide bonds. In the new patent application US20220344294, the **alignment problem is fixed** by a semiconductor devices with three-dimensional hybrid-bonding interconnect structures that include additional surface area for oxide bonding and facilitate mechanical alignment. Conventional solder interconnects for electrically coupling dies in a vertical stack can significantly increase the overall package height**. Hybrid bonding can reduce package height, but also has limitations**. The pending patent application US20220344270 provides **reliable die-to-die interconnections while avoiding the stringent alignment, surface cleaning, and planarization requirements associated with hybrid bonding approaches.**

- Regarding the IP activity on 3D-stacked memory dies, few new inventions were published this quarter (for a memory maker). One new invention discloses a process to **fabricate stacked memory dies without the use of TSV** (US20220375902). The method includes forming a reconstructed wafer or panel of memory known good dies and processing them with redistribution layer. Memory known good dies and RDL are then singulated and stacked, via holes are formed at locations extending beyond the lateral periphery of the semiconductor stack of dices. The new patent application US20230090919 discloses **power distribution for stacked memory** by implementing conductive paths for providing power to another memory die, where each conductive path may pass through the memory die but may be electrically isolated from circuitry for operating the memory die.

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SK Hynix
Q4-2022 IP ACTIVITY

SAMPLE

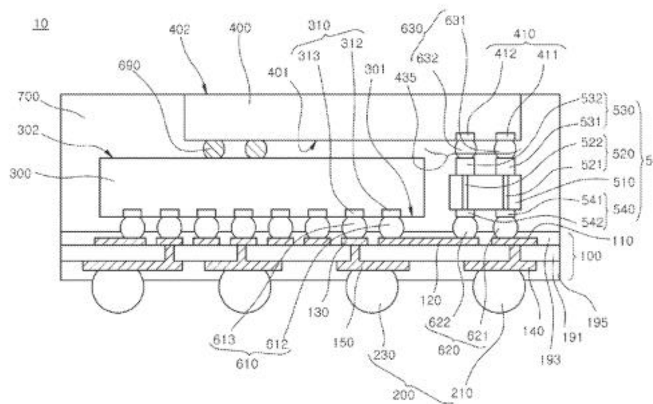
Note: A patent family/patent can belong to multiple segments.

	Q4 2022	SEGMENTS						
		All Fan-Out packaging	FO - Panel level	All 2.5D/3D packaging	Interposer / Bridge	Hybrid bonding	3D-stacked memory	Others
New patent families (inventions)	15	2		4	3	1		6
Patent families newly granted	10			2	2			7
Patents expired or abandoned	11							11

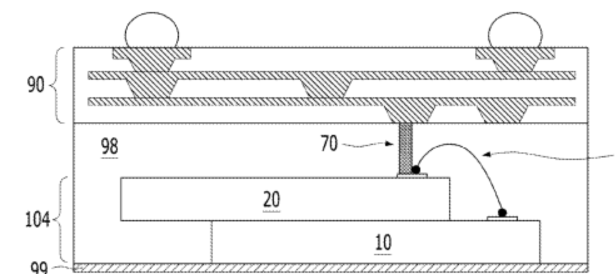
SK Hynix had a limited IP activity in Q4-2022. Main new inventions relate to chip stacking and connection between them.

This quarter, SK Hynix got a new granted patent US11495545 in which chip stacking and connection is achieved by using a **bridge die** (500) and RDLs.

In the new patent application US20220392866, a lower semiconductor die and an upper semiconductor die are stacked in a staircase form. The **electrical signal interference** among vertical wires is reduced because the vertical wires are disposed to be spaced apart from each other.



US20200273801



US20220392866

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YMTC

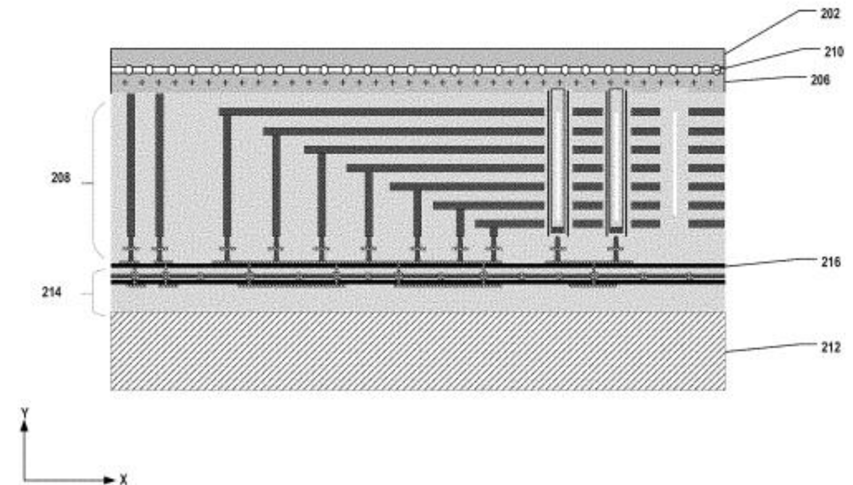
Q4-2022 IP ACTIVITY

Note: A patent family/patent can belong to multiple segments.

	Q4 2022	SEGMENTS						
		All Fan-Out packaging	FO - Panel level	All 2.5D/3D packaging	Interposer / Bridge	Hybrid bonding	3D-stacked memory	Others
New patent families (inventions)	25	1		2		2		22
Patent families newly granted	6			1		1		5
Patents expired or abandoned								

YMTC had a limited patent activity in Q4-2022.

Methods for forming 3D semiconductor devices are disclosed in the new patent application CN115497949. The first semiconductor structure comprises a first substrate and a first peripheral circuit (vertical transistors). The method further comprises **bonding the first peripheral circuit and a memory array**. Then **bonding the first semiconductor structure and the second semiconductor structure**. The second semiconductor structure comprises a second substrate and a second peripheral circuit arranged on the second substrate. Bonding may be performed for instance by **hybrid bonding** (YMTC signed a license agreement with Xperi in 2021).



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SAMPLE

NPE

(non-practicing entities)

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Xperi / Adeia

Q4-2022 IP ACTIVITY

SAMPLE

Note: A patent family/patent can belong to multiple segments.

	Q4 2022	SEGMENTS						
		All Fan-Out packaging	FO - Panel level	All 2.5D/3D packaging	Interposer / Bridge	Hybrid bonding	3D-stacked memory	Others
New patent families (inventions)								
Patent families newly granted	**5**			**5**	**3**	**5**		
Patents expired or abandoned	**16**							**16**

- **Xperi/adeia** is mainly protecting IP on **hybrid bonding for 3D stacking of dies and wafers**. The licensing company (a.k.a non-practicing entity, NPE) has licensed its DBI hybrid bonding related patents to main memory makers [1] (**Samsung, SK Hynix, Micron, YMTC**).
- This quarter, **Xperi/adeia** was granted for new patent related to **Hybrid bonding** applied to a variety of applications, like bonding reconstituted wafers (US11476213) or stacked 3D NAND (US11469214). **Bonding chips to the surface of a carrier to form a reconstructed wafer** can also be achieved by using a direct bonding technique, to avoid adhesive materials, if the chip has a plurality of conductive interconnections as claimed in the patent US11462419 newly granted this quarter. Finally, in the new granted patent US11538781, **Xperi/adeia** is looking at incorporating stress compensation elements, mounted to a carrier and at least partially embedded in the molding compound. The stress compensation element and the integrated device die are directly bonded to the carrier without adhesive.

[1] https://adeia.com/licensing/ (List of licensees as of January 5, 2023)

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ANNEX

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ANNEX

On-demand Q&A session on specific patented technologies or company IP portfolios

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Take advantage of direct interaction with our analysts by phone call and/or email

Q&A session and open discussion with our IP analysts (100h a year).

Asking for questions and/or requesting for specific patent search on company or technology.

Contact: contact@knowmade.fr

Examples:

- Could you tell me more about the patent portfolio of this company?
- What is exactly the invention claimed in these patents?
- Can you give me the patents filed by this company on these specific technologies?
- Can you shortly analyze the patents of this new entrant?
- What are the patents issued in Japan and Korea for this application?
- Please give me more details about this patent litigation.
- We want to file a new patent, can you help us to assess the prior-art in this field?
- I would like to invalidate these patents, could you do a prior-art search?
- Can you help me to identify in patents the technical solutions to solve this issue?
- I would like to assess my freedom of operating in USA, can you give me the granted US patents covering this technology?
- I am looking for free technologies I could use safely without infringing valid IP rights, can you give me newly expired patents related to this technology?

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ANNEX

Terminologies for Patent Analysis (1/2)

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Patent Applicant, Patent Assignee
An applicant is a person or organization (e.g. company, university, etc.) who/which has filed a patent application. An assignee is a person or organization (e.g. company, university, etc.) who/which holds patent rights. Patent applications may have more than one applicant/assignee.

Patent Family
A patent family is a set of applications or publications related to the same invention (different countries) and claiming the same priority(ies). All members of a patent family, except American continuation-in-part, share all their priorities.

Priority Date
The priority date is defined as the date on which the first patent application disclosing the invention was filed (up to 12 months before the filing of the application). The patent document is made available to the public about 18 months after the priority date (except if early publication is requested).

Priority Number
A priority number is the filing number of a priority document. The priority number is made up of a country code (two letters), the year of filing (two or four digits) and a serial number (variable, maximum seven digits).

Publication Date
The publication date is the date on which the patent application is published and is made available to the public, therefore entering into the state of the art.

First publication date
First publication date is defined as the earliest patent publication date disclosing the invention (herein “year of first publication”). The date or year of publication of a patent family must always read as the date or year of first publication.

Publication Number
The publication number is the number assigned to a patent application for the publication. Publication numbers are generally made up of a country code (two letters) and a serial number (variable, one to twelve digits).

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ANNEX

Terminologies for Patent Analysis (2/2)

SAMPLE

Citations

A citation is a reference made to a prior art document that is considered relevant to determine the patentability of a given invention. Citations are made by the applicant or by the office examiner during the examination of the patent application.

WO and EP Patent Applications

International (WO) and European (EP) patent applications are administered by the World Intellectual Property Organization (WIPO) and the European Patent Office (EPO), respectively.

- WO applications designate Contracting parties (official or non-official countries) of the Patent Cooperation Treaty (PCT) through their national or regional systems and will have the same effect as national or regional patent applications in each designated state or region, leading to a granted patent in each state or region. In this report, patent families are often designated by their funding PCT member. Entering into national phase of a PCT application can be checked on WIPO's Patentscope database.

EP applications are regional patent applications and may lead to granted EP patents upon validation in one or more designated Contracting States of the European Patent Convention (EPC) (i.e. 'bundle' of individual national patents). An EP granted patent can also be validated in Morocco, the Republic of Moldova, Tunisia and Cambodia and/or extended in Bosnia-Herzegovina, and Montenegro upon payment of an additional fee.

Legal Status of the Patent Document (patent or patent application)

Granted: Enforceable patent issued by a patent office after an examination process of a patent application.

Pending: Patent pending is the term used to describe a patent application that has been filed with the patent office, but has not yet been issued as a granted patent. Hence, the scope of protection of a pending application, or whether a patent will even be granted, is unknown.

Abandoned/Lapsed: A patent or patent application that is not enforceable anymore because the applicant withdrew his patent application, failed to respond to an office action during the examination, or did not pay the maintenance fees. Typical office status for Lapsed could be "abandoned", "lapsed", "withdrawn", "surrendered", etc.

Expired: A granted patent that is no longer in force as it has reached its maximum duration (in most countries: 20 years from the filing date, provided CCP or paediatric extension).

Rejected/Revoked: A patent or patent application that is not enforceable before the end of the normal term for patentability-related reasons.

- The status "rejected" mainly refers to a pre-grant patent application for which a grant decision has been denied (e.g. due to a lack of patentability of the invention).
- The status "revoked" mainly refers to a formerly granted patent that have been later cancelled by an office (e.g. following an Opposition, a Post Grant Review or an Inter Partes Review) or a court. Typical office status for "Revoked" could be "suspended", "interrupted", "cancelled", "revoked", "refused", etc.

International Patent Classification (IPC)

The technical content of patent documents is classified in accordance with the International Patent Classification (IPC). The publishing office assigns an IPC symbol valid at the time of publication of the patent application. The complete IPC can be found on the website of the World Intellectual Property Organization (WIPO - http://www.wipo.int/ipcpub).

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