

# TSV STACKED MEMORY Patent Landscape Analysis

An emerging market with leading industrials and first patent litigations;

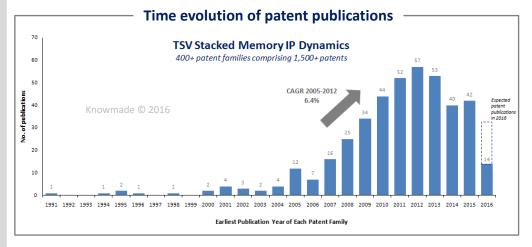
Who owns what?

# A FAST GROWING TSV MEMORY MARKET

In the semiconductor industry, 3D integration using through-silicon via (TSV) has been considered to be a promising way for improving performance and density instead of conventional device scaling. By connecting stacked chips with the TSV vertical connections, the wide bandwidth I/O and reduction of interconnects length can be achieved. Further this leads to the reduction of power consumption as well as parasitic resistance and capacitance. The last 2 years have seen some changes on the TSV memory market with first products appearance (3DS DDR4, HBM, HMC) but also first hot patent litigations between ELM 3DS and microelectronics giants (Samsung Electronics, SK Hynix and Micron Technology). The TSV 3D Memory market to show 43% CAGR to 2020 according to Yole Development, with almost 200K units wafers in 2016.

Samsung started 3DS DDR4 DRAM production in 2014, HBM2 4Gb at the beginning of the year and 8Gb will be introduced later this year. For 2019-2020, Samsung predicts on two future paths: HBM3 with higher capacity and higher bandwidth and low cost HBM (with significant cost savings arrive from the narrower width allowing for simpler memory stacks with less TSVs). SK Hynix entered in production of HBM1 2Gb in 2014 for graphic and cache applications and will commence mass production of HBM2 4Gb in Q3 2016 and 8Gb in Q4 2016 for HPC and server use. SK Hynix started also production of 3DS DDR4 8Gb and Wide I/O2 in 2015. SK Hynix predicts a wider array of purposes for tomorrow new HBM generation. Micron Technology began production of 16Gb HMC Gen2 in 2014 and will start production of HMC Gen3 in 2017. Those products get from low-end applications like networks servers (3DS DDR4) up to high-end computing applications (HMC, HBM).

Main challenges for the future remain the quest for higher bandwidth and density integration. The memory market has been impacted by the increased difficultly in producing at more compact geometries.



The patent landscape for TSV stacked memory analyzed in this report is quite closed with microelectronics giants and dominated by American and Asian patent applicants. The USA and Korea represent the main countries of patent fillings, while Europe seems to represent only few interest for patent applicants. First patents involving TSV stacked memories were already published in the 1990s, but the development of the technology really started in the mid-2000s with a significant increase of patent publications since then. To this date, more than 400 patent families relating to TSV stacked memory technology have been published. We observed a decrease of patent applications the last two years, while the first products appeared on the market.

# **REPORT OUTLINE**

- TSV Stacked Memory
- Patent Landscape Analysis
- September 2016
- PDF (140+ pages)
- Excel file (1,500+ patents)
- €5,990 (Multi-user license)

# **KEY FEATURES OF THE REPORT**

- IP trends including time evolution of patent publications and patent filings countries
- Current legal status of patents (granted, pending application, abandoned, expired)
- Main patent assignees (ranking, time evolution, geographical coverage)
- Joint developments and IP collaboration network of main patent assignees
- Key patents
- Profile of 5 key players (Samsung, Toshiba, Micron Technology, SK Hynix, Intel), including:
  - Technology and market data for TSV stacked memory
  - Key patents
  - Cross link analysis between teardown analysis, process flow and owned patents for each critical process points
  - **Technical challenges** and relevant solutions found in the patents: error repair, multi-channel package, thermal dissipation, alignment accuracy, connection failure
  - Patent litigations (ELM 3DS vs SK Hynix/Micron/Samsung)
- Excel database with all patents analyzed for the 5 key players, including technology segmentation

# **RELATED REPORTS**

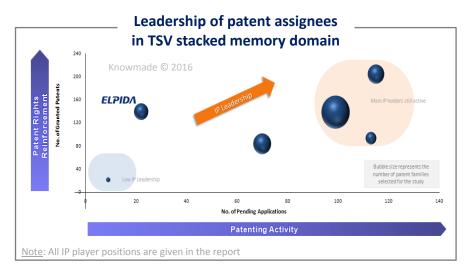
- 3DIC and 2.5D TSV Interconnect for Advanced Packaging: 2016 Business Update (Yole Développement)
- AMD High-Bandwidth Memory (SystemPlus Consulting)
- Samsung 3D TSV Stacked DDR4 DRAM (SystemPlus Consulting)



# **KNOW THE IP POSITION OF KEY PLAYERS**

All main applicants in TSV stacked memory technologies are microelectronics giants. Most of them are American or Asian. Interestingly, key patented technologies on TSV stacked memories are hold by American and Asian microelectronics giants (Samsung, SK Hynix, Micron/Elpida, Intel) but also small companies (ELM 3DS, Besang).

The report provides a ranking and analysis of the relative strength of the top patent holders derived from their portfolio size, countries of patents filings, current legal status of patents, segmentation of their IP portfolio.



The 5 major players (Samsung, Toshiba, Micron/Elpida, SK Hynix, Intel) have been profiled, and for each of them this report provides detailed: patent portfolio analysis with technology and market data, key patents, IP strategies, technical challenges and relevant solutions found in the patents, cross link analysis between marketed products and owned patents for each critical process points. Moreover, the report provides a detailed analysis of the patent litigations ELM 3DS vs SK Hynix/Micron/Samsung.

# Cross link analysis between teardown/flow chart/patent for each critical process points The package structure includes 4 stacked dies, TSV & microbumps for die connection, flip chip bumps for package connection. \*\*Backage structure includes 4 stacked dies, TSV & microbumps for die connection, flip chip bumps for package connection. \*\*Backage structure includes 4 stacked dies, TSV & microbumps for die connection, flip chip bumps for package connection. \*\*Backage structure includes 4 stacked dies, TSV & microbumps for die connection, flip chip bumps for package connection. \*\*Backage structure includes 4 stacked dies, TSV & microbumps for die connection, flip chip bumps for package connection. \*\*Backage structure includes 4 stacked dies, TSV & microbumps for die connection, flip chip bumps for package connection. \*\*Backage structure includes 4 stacked dies, TSV & microbumps for die connection, flip chip bumps for package connection. \*\*Backage structure includes 4 stacked dies, TSV & microbumps for die connection, flip chip bumps for package connection. \*\*Backage structure includes 4 stacked dies, TSV & microbumps for die connection, flip chip bumps for package connection. \*\*Backage structure includes 4 stacked dies, TSV & microbumps for die connection, flip chip bumps for package connection. \*\*Backage structure includes 4 stacked dies, TSV & microbumps for die connection, flip chip bumps for package connection. \*\*Backage structure includes 4 stacked dies, TSV & microbumps for die connection, flip chip bumps for package connection. \*\*Backage structure includes 4 stacked dies, TSV & microbumps for die connection, flip chip bumps for package connection. \*\*Backage structure includes 4 stacked dies, TSV & microbumps for dies connection, flip chip bumps for package connection. \*\*Backage structure includes 4 stacked dies, TSV & microbumps for dies connection. \*\*Backage structure includes 4 stacked dies, TSV & microbumps for dies chip bumps for package connection. \*\*Backage structure includes 4 stacked di

# CROSS-LINK ANALYSIS DEVICES/PATENTS

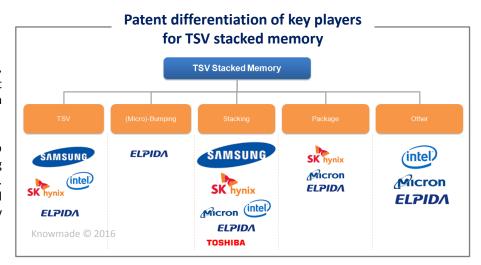
The cross-link analysis provides key patents of each critical process points (package, stack, interconnections) matching the teardown of TSV memory devices (HBM, 3DS DDR4, HMC or TSV NAND Memory) of key players.

The deep analysis of the patent portfolios held by key players includes a point on relevant technologies for future developments of TSV stacked memories. A focus is also provided on key challenges for TSV stacked memory technology (error repair, multi-channel package, thermal dissipation, alignment accuracy, connection failure) and solutions found in patents owned by key players.

# **IP LITIGATION DEEP ANALYSIS**

In 2014, with first products appearance (HBM, 3DS DDR4), ELM 3DS filed actions for patent infringement against defendants SK Hynix, Micron Technology and Samsung Electronics.

This report provides a complete and deep understanding of IP litigation history including litigated patents families and inter-partes reviews. The analysis includes also status of the cases and prior art analysis before ELM's patents priority date.



# **USEFUL PATENT DATABASE**

Our report also includes an Excel database containing all of the analyzed patents (1,500+ patents). This database allows multi-criteria searches and includes patent publication number, hyperlinks to the original documents, priority date, title, abstract, patent assignees and legal status for each member of the patent family.



# **ASSIGNEES CITED IN THE REPORT** (NON-EXHAUSTIVE)

Samsung Electronics, Micron Technology, Elpida Memory, Intel, SK Hynix, Toshiba, AMD, Hitachi, NEC, Hewlett Packard, IBM, Rambus, ELM 3DS, TSMC, SanDisk ...

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# TSV Stacked Memory Patent Landscape Analysis

September 2016

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- 2.2 Some weeks prior to the release date the Seller can propose a pre-release discount to the Buyer.

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BIC or SWIFT code: CCBPFRPPNCE

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- 4.4 All the information contained in the Products has been obtained from sources believed to be reliable. The Seller does not warrant the accuracy, completeness adequacy or reliability of such information, which cannot be guaranteed to be free from errors.
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- 4.6 In the case where, after inspection, it is acknowledged that the Products contain defects, the Seller undertakes to replace the defective products as far as the supplies allow and without indemnities or compensation of any kind for labor costs, delays, loss caused or any other reason. The replacement is guaranteed for a maximum of two months starting from the delivery date. Any replacement is excluded for any event as set out in article 5 below.
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