TSV Stacked Memory

Patent Landscape Analysis

September 2016

KnowMade
IP and Technology Intelligence

2405 route des Dolines, 06902 Sophia Antipolis, France
contact@knowmade.fr
http://www.knowmade.com

TABLE OF CONTENTS

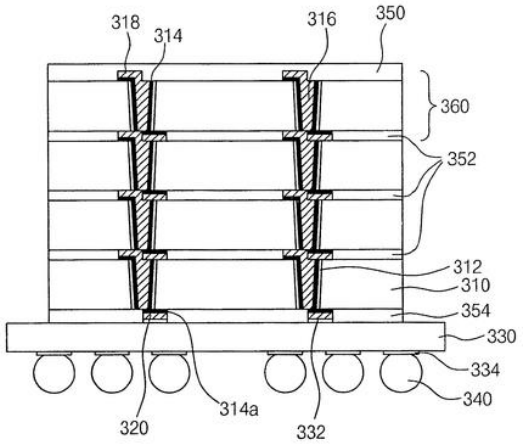
INTRODUCTION

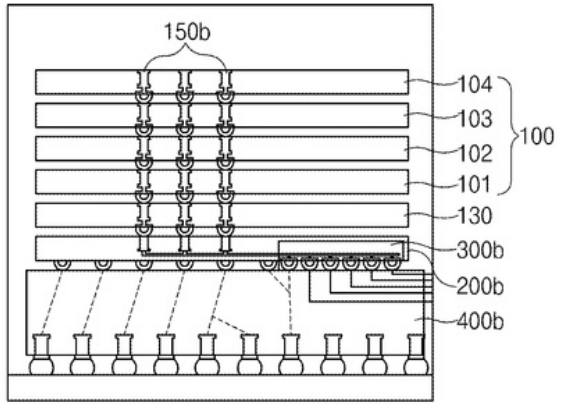
Scope of the Report

- This report provides a detailed picture of the patent landscape for **TSV Stacked Memory**, with 3-dimensional structu
- This report covers **patents published worldwide up to June 2016**.
- We have selected and analyzed more than **1,500 patents** split in more than **400 patent families** relevant to the scope of this report.

Included in the report

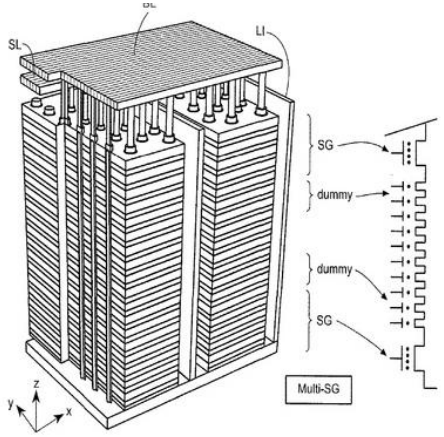
- *Any patent describing a **3D stacked memory using TSV** (Through Silicon Via).*
- *Patents mentioning **package** of these **TSV memory** dies or chips.*

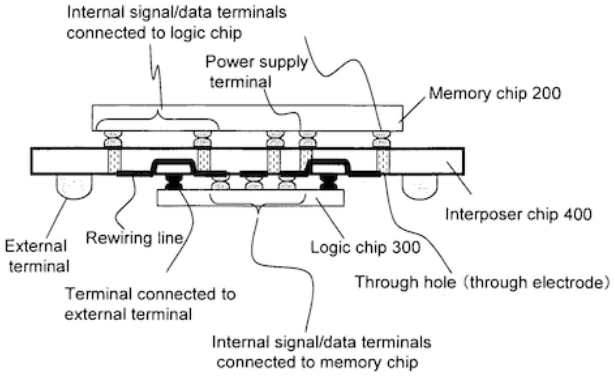




Not included in the report

- *Patents with stacked memory **without TSV** (Through Silicon Via).*
- *Patents with memory that are **not in a 3-dimensional structure**.*
- *Patents with stacked **memory used in a device**.*
- *Patents with stacked **memory using wire connection.***





METHODOLOGY

Patent Search, Patent Selection, Patent Analysis (1/2)

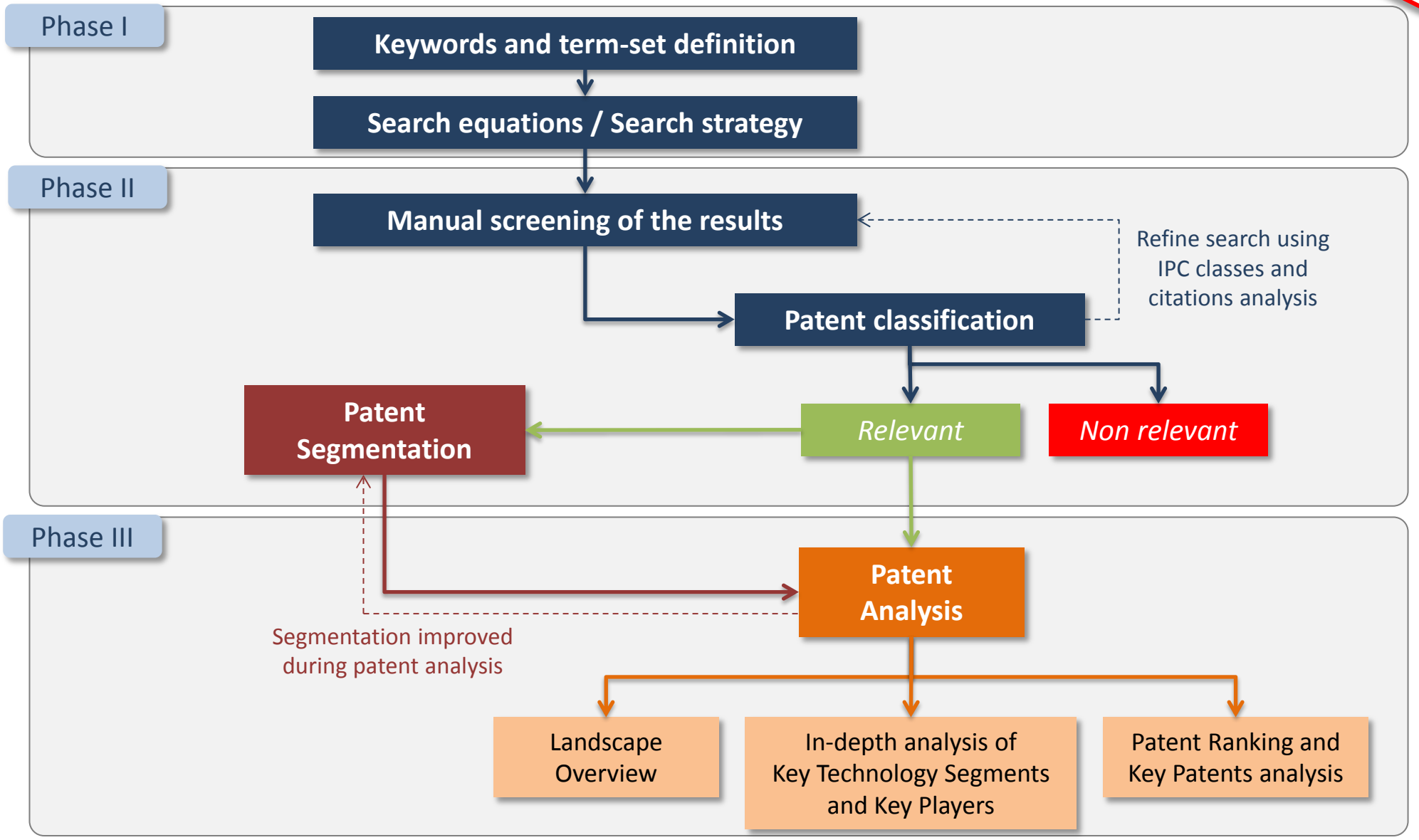
- The data were extracted from the **FamPat worldwide database** (Questel-ORBIT) which provides 80+ million patent documents fr 95 offices.
- The search for patent was performed in **June 2016** hence patents published after this date will not be available in this report.
- The patents were grouped by **patent family**. A patent family is a set of patents filed in multiple countries to protect a single invention by a common inventor(s). A first application is made in one country – the priority country – and is then extended to other countries.
- The selection of the patents has been done both automatically and manually (all details in next slides).

Number of selected patent families for the TSV Stacked Memory Patent Landscape Analysis:
417 over a number of returned results > 4,000

- The statistical analysis was performed with **Orbit IP Business Intelligence web based patent analysis software from Questel**.
- The patents were **manually categorized in technical segments** using keyword analysis of patent title, abstract and claims, in conjunction with expert review of the subject-matter of inventions (all details in next slides).
- For legal status of European (EP) and PCT (WO) patent applications, EPO Register Plus has been used. For legal status of US patents, USPTO PAIR has been used. For legal status of other patents, information have been gotten from their respective national registers.

METHODOLOGY

Patent Search, Patent Selection, Patent Analysis (2/2)



METHODOLOGY

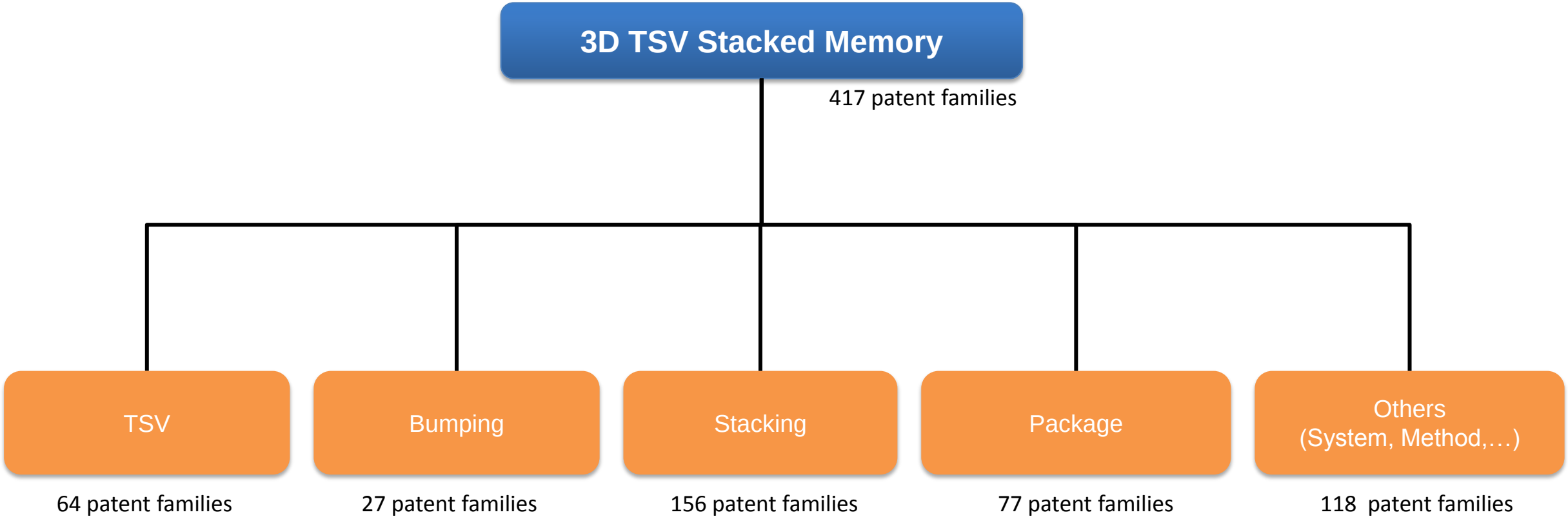
Search Equations

	STEP	SEARCH EQUATION	
Patents related to Memory	**Step-1**	(MEMORY OR MEMORIES OR ?SRAM? OR ?DRAM? OR ?NAND? OR ?NOR? OR +NVM+ OR ?FERAM? OR FERROELECT+ RAM OR FERROELECT+ RANDOM ACCESS MEMOR+ OR ?STT-RAM? OR ?MRAM? OR MAGNET+ RAM OR MAGNET+ RANDOM ACCESS MEMOR+ OR ?PCRAM? OR (PHASE_CHANGE 3D MEMOR+) OR PHASE CHANGE RANDOM ACCESS MEMOR+ OR ?R_RAM? OR ?RERAM? OR ?CBRAM? OR ?OXRAM? OR RESIST+ RAM OR RESIST+ RANDOM ACCESS+ MEMOR+ OR RESIST+ NON_VOLATIL+ MEMOR+ OR CONDUCTIVE BRIDGE RANDOM ACCESS+ MEMOR+ OR OXIDE RESISTIVE RANDOM ACCESS+ MEMOR+ OR CONDUCTIVE BRIDGE MEMOR+ OR OXIDE RESISTIVE MEMOR+ OR RESISTIVE MEMOR+ OR PROGRAMMAB+ METALLIZAT+ CELL+ OR (RESIST+ CHANG+ 3D MEMOR+) OR (RESIST+ 3D MEMOR+) OR ?MEMRIST+)/BI	>1,000,000
Patents related to TSV Memory	**Step-2**	**Step-1** AND ((THROUGH 1D (SILICON? OR SUBSTRATE? OR WAFER? OR GLASS+) 1D (VIA? OR HOLE? OR INTERCONNECT+)) OR (THROUGH 0W HOLE 0W (VIA? OR INTERCONNECT+)) OR (THROUGH 0W VIA 0W (HOLE? OR INTERCONNECT+)) OR ((THROUGH 0W WIRE) 0W INTERCONNECT+) OR TSV? OR TSV-BASED)/BI/CLMS	>800
Patents related to Memory Manufacturing Process	**Step-3**	**Step-1** AND (MICRO_BUMP? OR MICRO_PADS OR FLIP_CHIP+ OR COPPER PILLAR? OR CU PILLAR? OR CU-CU OR INTERPOSERS OR TRANSPOSER? OR UNDER_FILL+ OR ((((CARRIER+ OR HOST+ OR HANDL+ OR SUPPORT+ OR BOND+) 2D (TEMPO+ OR PROVISIO+ OR GLASS)) OR (BONDING OR DE_BONDING)) 2D (PACKAGE? OR DIE? OR CHIP?)) OR ((THIN+ OR SLIM+ OR CMP OR POLISH+ OR GRIND+) 2D (WAFER? OR SUBSTRATE?)))/BI/CLMS	>3,000
Patents related to Memory Stacking	**Step-4**	**Step-1** AND **Step-2**/DESC AND (+stack+ OR pile OR piled OR piling OR pile_up)/BI/CLMS	>1,000
Automatically and manually selection	**Step-5**	**Step-2** OR **Step-3** OR **Step-4**	>4,300
		Relevant patent families selected for the study	**417**

METHODOLOGY

Segmentation of Patents

Patents selected for the study were manually categorized into following segments.

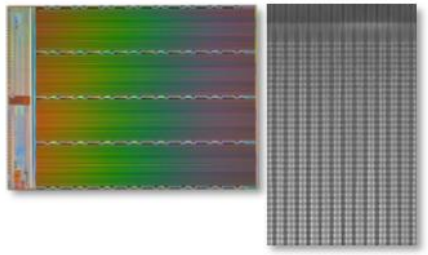


TECHNOLOGY OVERVIEW

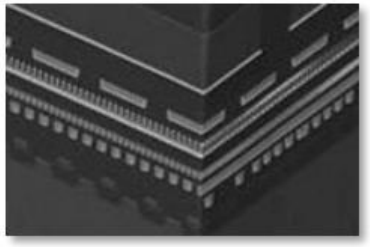
3D Integration Memory

The 3D approach can be done at two levels:

• **Front-end (silicon) approach**: Memory cells are vertically organized, not horizontally. Monolithic 3D wafers are manufactured all in one fab, and rather than stacking 2 or more wafers, a base wafer is used onto which additional layers of crystallized silicon and metalized layers are added using traditional fab equipment. This approach is used for 3D NAND (also called VNAND by Samsung), and is not possible with DRAM.



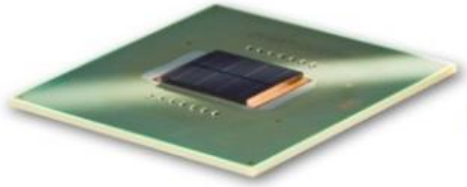
3D NAND



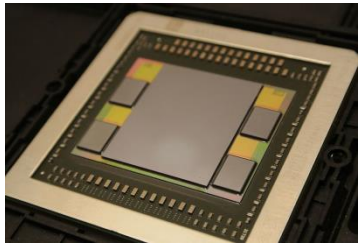
Cross-Point Memory

3D Memory without TSVs will be the focus of a next IP report

• **Back-end (packaging) approach**: Memory chips are stacked and connected with 3D assembly technologies like TSV (through silicon vias). 3D TSVs involve taking two finished device wafers (either from the same or different fabs) and vertically interconnecting them at the chip level with through silicon vias (TSVs) in either wafer-to-wafer or die-to-wafer processes. This approach is used for DRAM with HMC and HBM techniques.



Hybrid Memory Cube



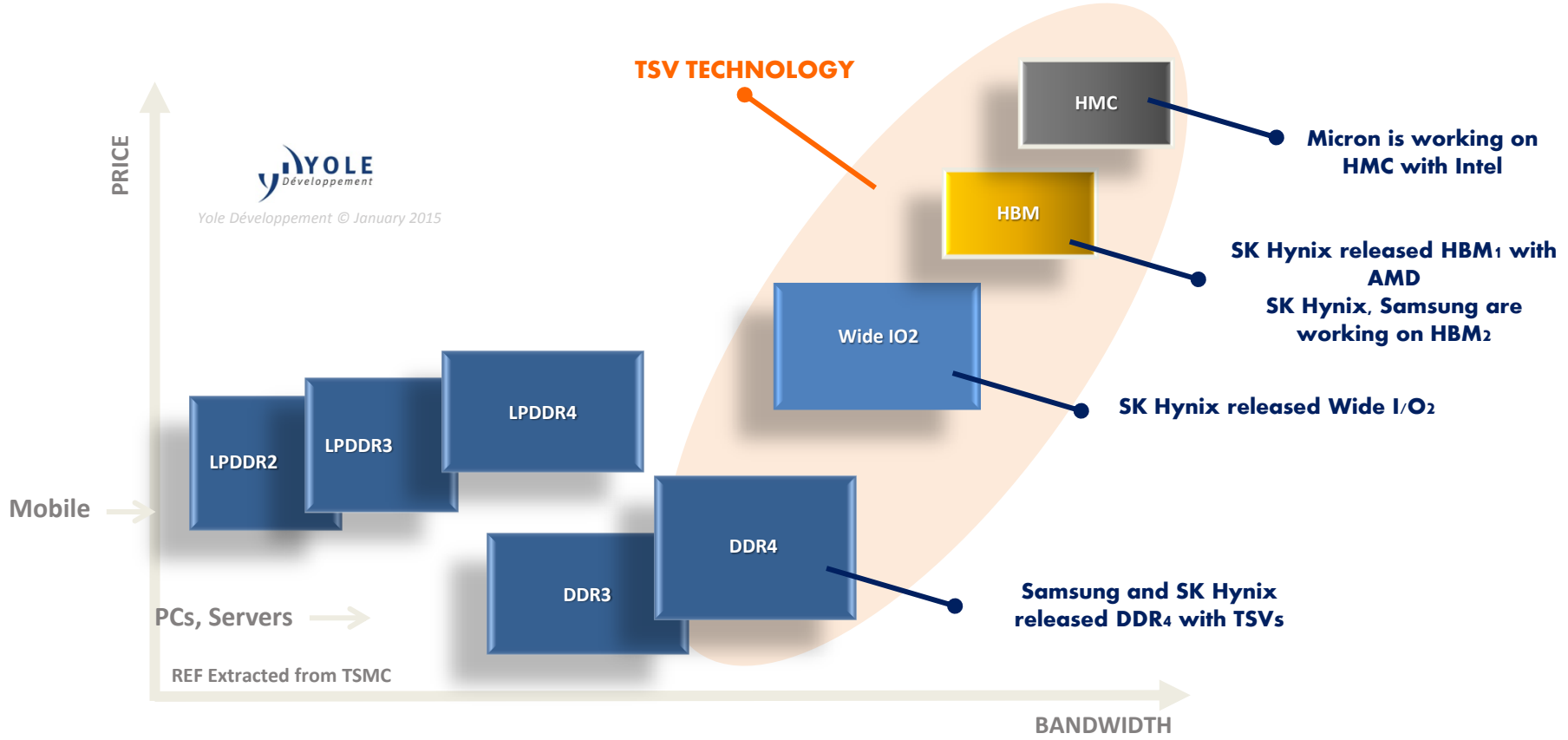
High Bandwidth Memory

In this study, we focus on 3D Memory Package Technology with TSVs

TECHNOLOGY OVERVIEW

3D Packaging TSV Approach

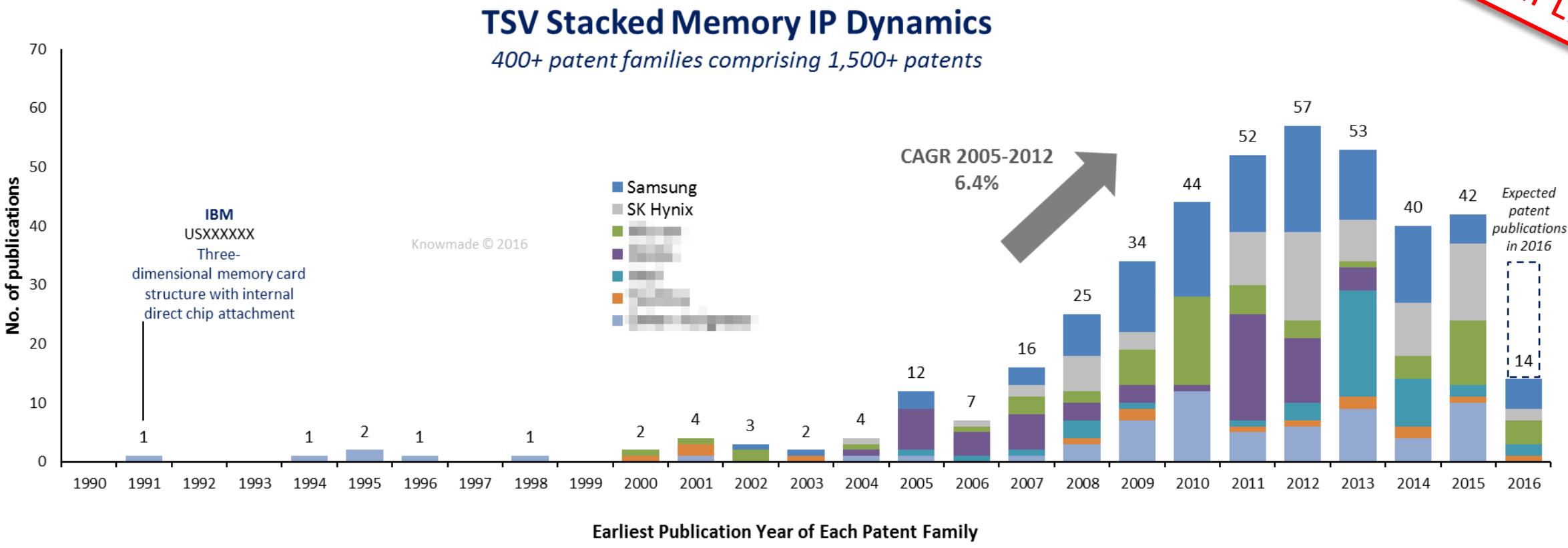
3D packaging Through Silicon Via (TSV) approach is used in different offers (DDR4, Wide IO, HBM, HMC) in order increase bandwidth and bit density. Those offers get from low-end applications like networks servers (DDR4) up to high-end computing applications (HMC, HBM).



Bandwidth is the most important challenge of DRAM

PATENT LANDSCAPE ANALYSIS

Time Evolution of Patent Publications



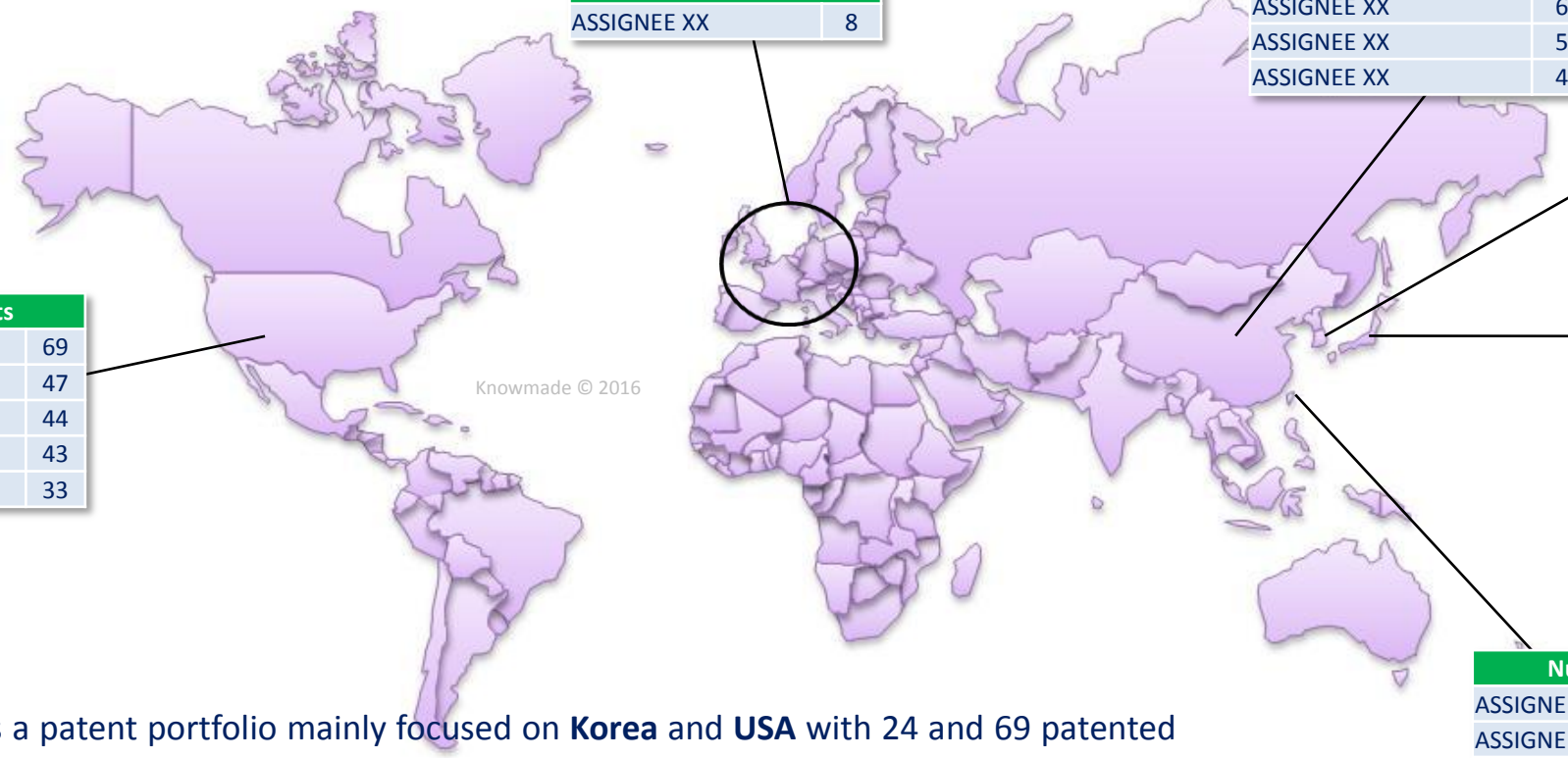
Note: The patent search was done in June 2016, thus the data corresponding to the year 2016 are not complete. At the time of the patent search, 14 patent families had been published in 2016.

- First patents involving TSV stacked memories were already published in the 1990s (USXXXXX, IBM), but the development of the technology really started in the mid-2000s with a significant increase of patent publications since then.
- To this date, more than 400 patent families relating to TSV stacked memory technology have been published. We observed a decrease of patent applications the last two years, while the first products appeared on the market (Wide I/O, HBM, DDR4 …).

PATENT LANDSCAPE ANALYSIS

Mapping of Main Current Patent Holders

Number of patent families containing granted patents in the corresponding country.



China

Number of grants	
ASSIGNEE XX	20
ASSIGNEE XX	11
ASSIGNEE XX	9
ASSIGNEE XX	6
ASSIGNEE XX	5
ASSIGNEE XX	4

Europe

Number of grants	
ASSIGNEE XX	8

Korea

Number of grants	
ASSIGNEE XX	24
ASSIGNEE XX	18
ASSIGNEE XX	15
ASSIGNEE XX	13

USA

Number of grants	
ASSIGNEE XX	69
ASSIGNEE XX	47
ASSIGNEE XX	44
ASSIGNEE XX	43
ASSIGNEE XX	33

Japan

Number of grants	
ASSIGNEE XX	33
ASSIGNEE XX	15
ASSIGNEE XX	10
ASSIGNEE XX	7
ASSIGNEE XX	6
ASSIGNEE XX	5

Taiwan

Number of grants	
ASSIGNEE XX	20
ASSIGNEE XX	23
ASSIGNEE XX	3
ASSIGNEE XX	3
ASSIGNEE XX	2
ASSIGNEE XX	2

- **Assignee XX** has a patent portfolio mainly focused on **Korea** and **USA** with 24 and 69 patented inventions in force respectively.
- Among the main assignees, **Assignee XX** shows the most **worldwide IP strategy** with a lot of granted patents in all geographic areas. **Assignee XX** patent portfolio has the **strongest position** in the map of granted patents.
- **Assignees XX** have no enforceable patents in **the European area**.

PATENT LANDSCAPE ANALYSIS

Summary of Assignees's Patent Portfolio

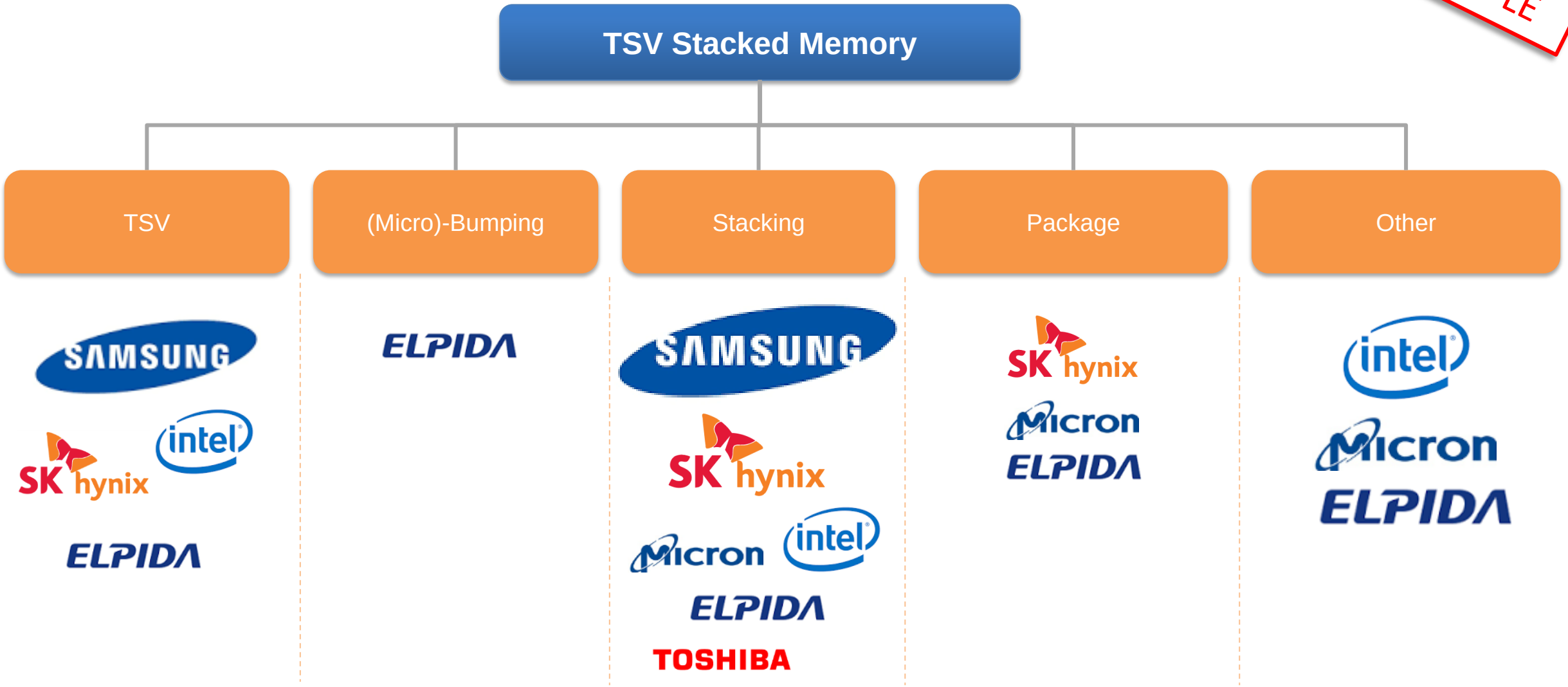
Patent Applicants	No. of patent families	Oldest priority date of the portfolio	No. of patent families filed / year (average)	No. of patent members	No. of patents / family (average)	Patent average age (year)	% of granted patents	% of pending patent applications	% of dead patents (rejected, lapsed, expired)	No. of alive patents / Family (granted, pending)	No. of granted patented by country					
											US	EP	JP	CN	TW	KR
COMPANY XX	XX	20XX	XX	XX	XX	4	XX%	XX%	XX%	XX	69	-	7	6	3	24
COMPANY XX	XX	2002	XX	XX	XX	XX	XX%	36%	XX%	XX	43	-	5	11	2	15
COMPANY XX	63	19XX	XX	337	XX	XX	XX%	XX%	XX%	XX	44	8	15	20	23	18
COMPANY XX	XX	20XX	4.2	XX	XX	XX	XX%	XX%	19%	XX	47	-	33	9	2	2
COMPANY XX	XX	20XX	XX	XX	5.2	XX	XX%	XX%	XX%	5.0	33	-	10	5	20	13
COMPANY XX	XX	19XX	XX	XX	XX	XX	46%	XX%	XX%	XX	7	-	6	4	3	1

highest value in column lowest value in column

- The top-6 of the main patent assignees owns more than 80% of the whole patent families, with most portfolios including more than 40 families each.
- The IP leaders are **XX** and **XX**. **XX** holds the largest patent portfolio in the TSV Stacked Memory with 117 patent families (comprising 539 patents) thanks to the acquisition of **XX** in 2013. **XX** has a worldwide IP strategy and should improve its presence in Europe in the next years.
- **XX** owns over 80% of alive patents (138 granted patents and 99 pending patent applications) and is strongly active in the USA and Korea. With 109 patent families (comprising 280 patents), **XX** holds the 2nd largest portfolio in the domain.

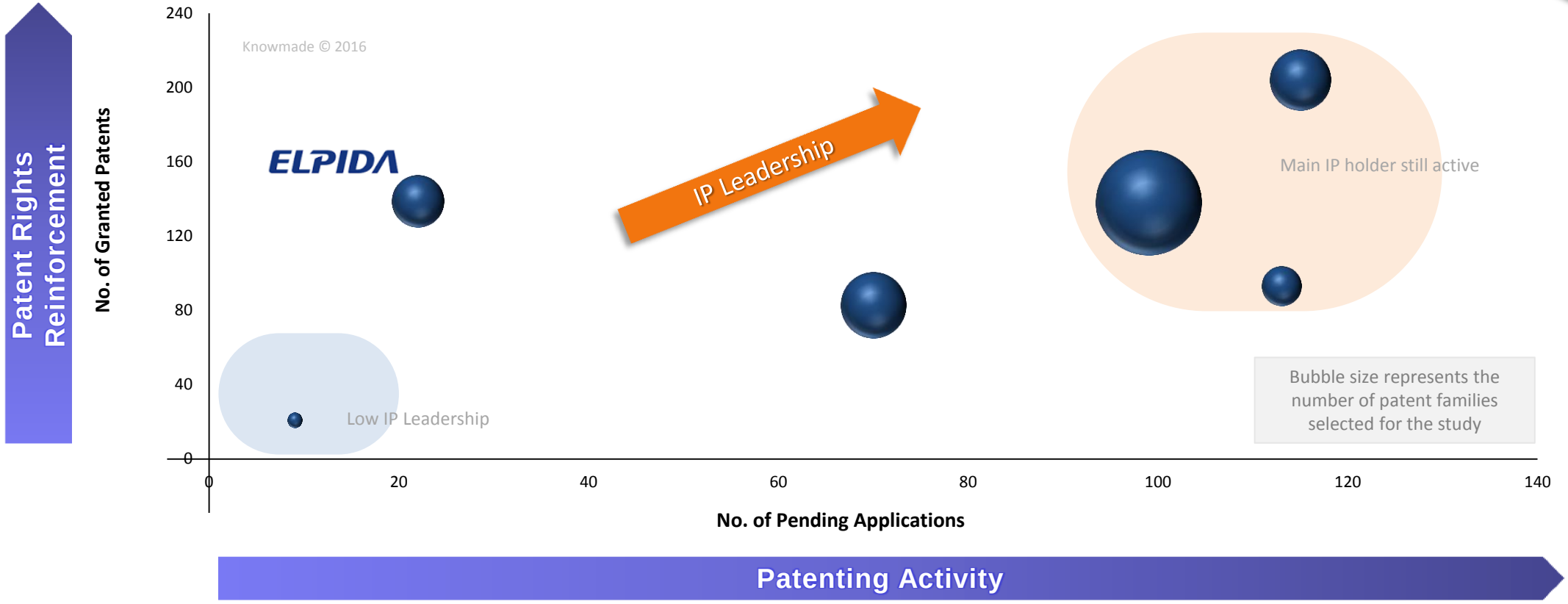
PATENT LANDSCAPE ANALYSIS

Patent Segmentation



PATENT LANDSCAPE ANALYSIS

IP Leadership of Patent Assignees

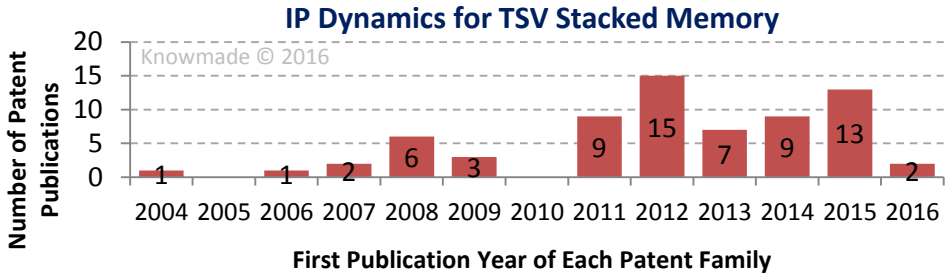


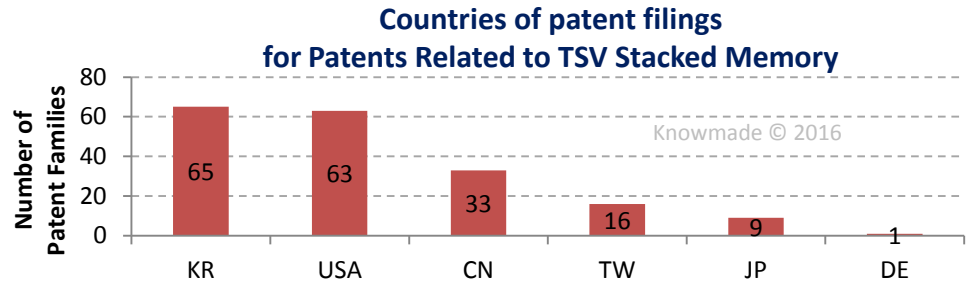
- **XX** shows a strong IP leadership. The company combines a high number of granted patents with a lot of pending patent applications.
- **XX** and **XX** have a significant leadership. Both own a large granted patent portfolio and are still active in terms of patent filings.
- **XX** could see its IP leadership increase in the future, considering their current patenting activity.

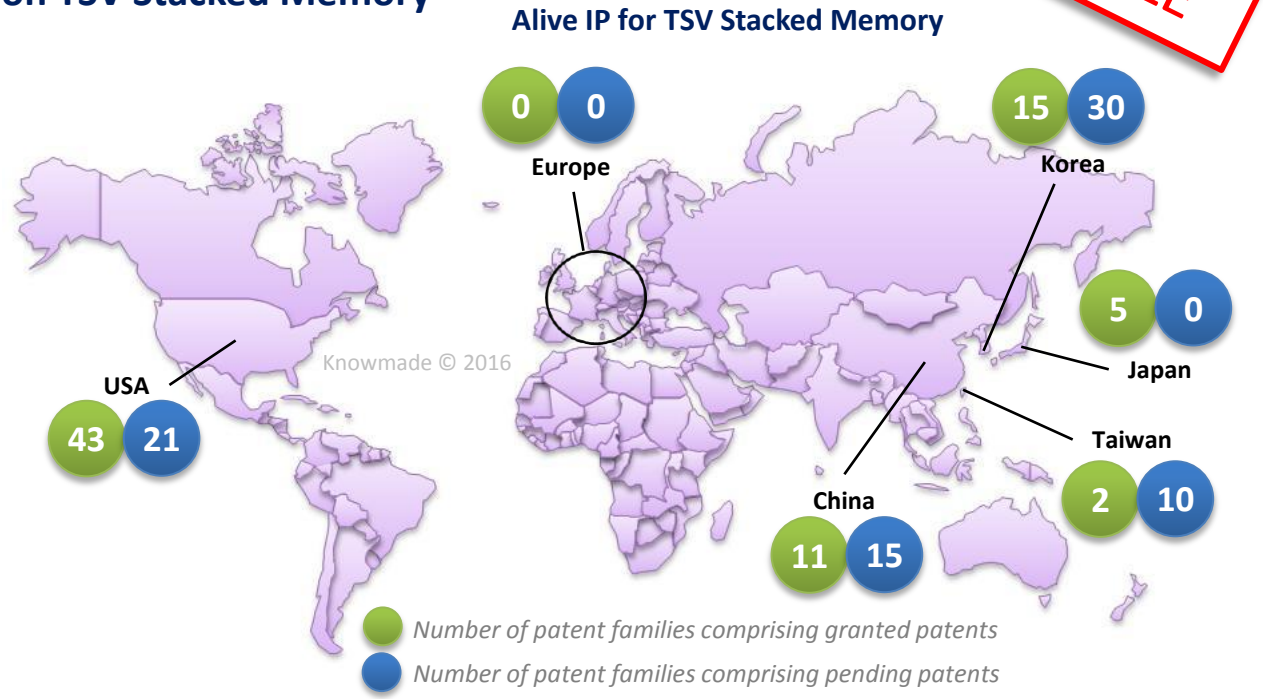
Key Player XX

Patent Portfolio Overview

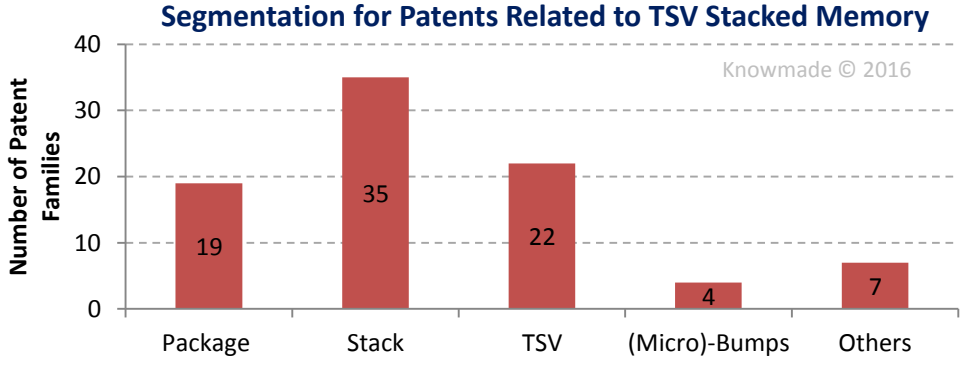
197 patents within 68 patent families on TSV Stacked Memory







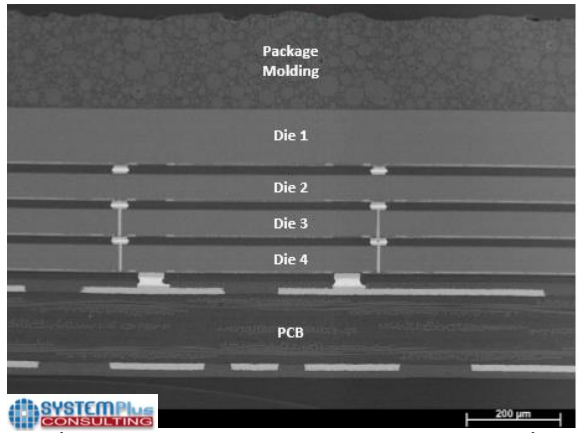
- Patent publications in 2008 rely on chip stack structure with through-silicon vias, in order to overcome the problems caused in the stack package using the metal wires, prevent the electrical characteristics of the stack package from deteriorating and enable miniaturization of the stack package. They describe solutions to absorb thermally-induced stresses, prevent warpage and cracks and improve operation.
- XX enters production in end 2000s and joined in 2011 YY program.
- In 2011-2015, XX was actively working on different kind of solutions: heat dissipation, adhesion, error failure,… in the memory stack.
- XX doesn't have a worldwide IP strategy in 3D TSV Memory. Indeed, XX has no alive patents in Europe and very few granted patents in Japan and Taiwan. However the high number of pending patent applications in Taiwan, but also Korea, China or USA will increase the number of granted patents in these countries in the future. XX has strong IP presence in USA.



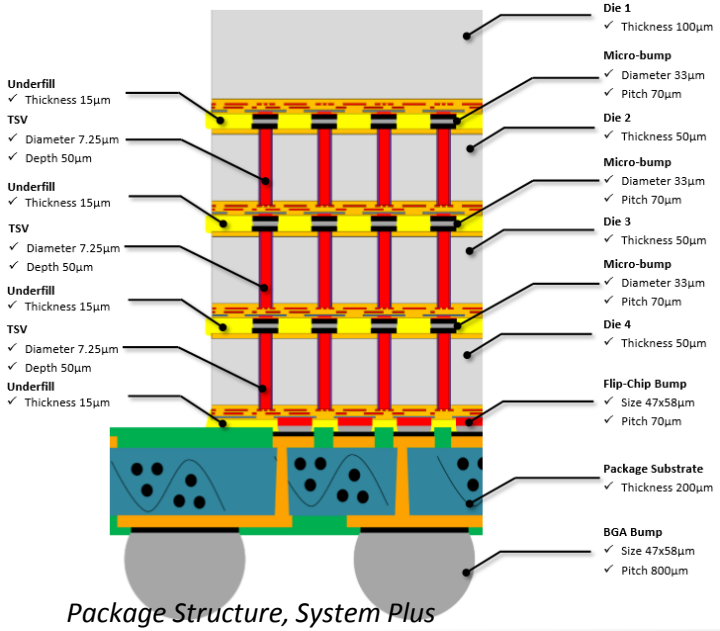
Key Player XX / Teardown Analysis and Related Patents

3D DDR4 - Package

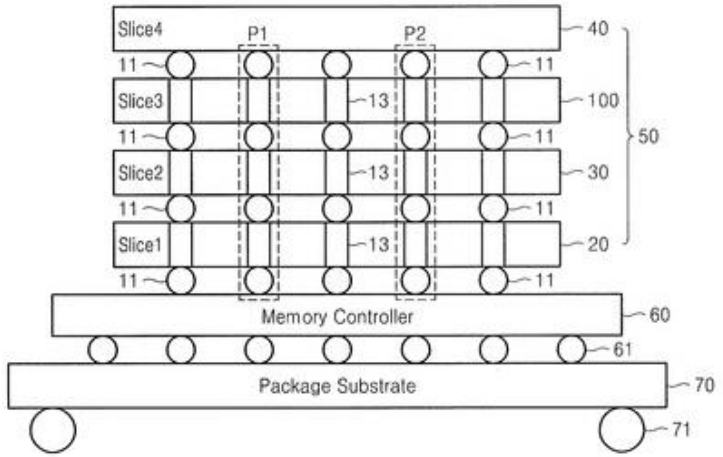
The package structure includes 4 stacked dies, TSV & microbumps for die connection, flip chip bumps for package connection.



Package Cross Section, SEM View, System Plus

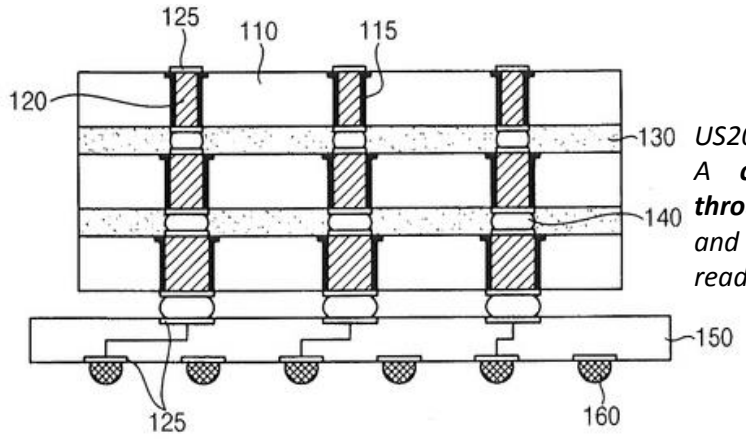


Package Structure, System Plus



US2014XXXXXX (2014)

*A stacked memory device includes a plurality of **a plurality of memory chips**; a first path to transmit a command signal to at least one of the plurality of memory chips; and a second path coupled to the plurality of memory chips, the second path to transmit a refresh control signal for controlling a refresh operation of at least one of the plurality of memory chips.*

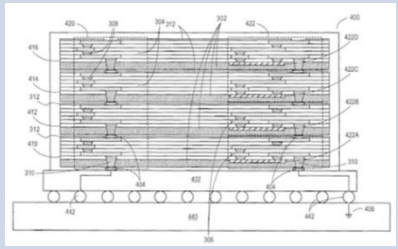
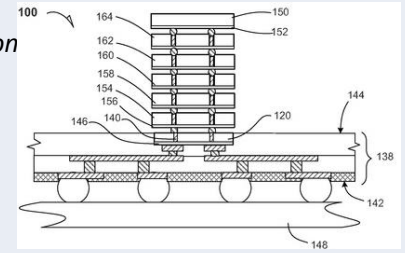
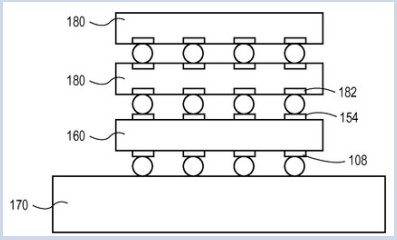


US2013XXXXXX (2013)

*A **chip stack package where a plurality of through silicon vias** are efficiently and readily aligned and a capacitance of a signal path is efficiently and readily adjusted.*

Key Player XX

Key Patent Families

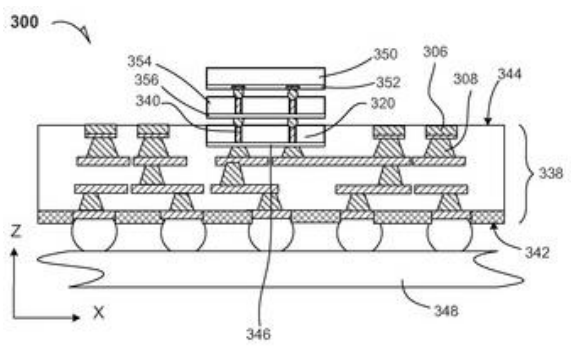
KEY PATENT FAMILIES *Patent number (representative member), earliest publication date, title and principal drawing*	RATIONALES FOR CHOICE *Refer to slide 18 for selection criteria*
USXXXXXX (2002) *Method and apparatus for generating a device id for stacked devices* 	- Future memory devices may utilize new technologies in packaging stacked devices, such as through-silicon vias or optical technology. The conventional method of bonding out a unique device ID for each stacked device, as described above, may not be practical for future device stacking technologies. - The present invention provide a method and apparatus for generating a unique device identifier (device ID) for each addressable integrated circuit (IC) device in a multi-die package, such as a stacked-CSP (chip scale package). - More than 32 citations per year on average (mostly by TSMC) - 1 US granted patent, 40+ claims
USXXXXXX (2012) *Die-stacking using through-silicon vias on bumpless build-up layer substrates including embedded-dice, and processes of forming same* 	- Disclosed embodiments relate to semiconductor microelectronic devices and processes of packaging them. - More than 7 citations per year on average (mostly by Micron Technology and Samsung Electronics) - Extended family (TW, US, CN, WO) - 3 granted patents (US, CN, TW), 40+ claims
USXXXXXX (2013) *3d interconnect structure comprising through-silicon vias combined with fine pitch backside metal redistribution lines fabricated using a dual damascene type approach* 	- Embodiments of the invention describe a 3D interconnect structure and process which combines through-silicon vias (TSVs) with very fine pitch backside metal redistribution layers (RDLs) using a dual damascene type process flow. This particular combination may allow for the physical locations of the TSVs to be decoupled from the chip-to-chip landing pad locations, thus providing greater circuit layout flexibility. In this manner multiple RDLs can be run between adjacent landing pad rows or columns. - Extended family (KR, US, CN, TW) - 2 granted patents (KR, US)

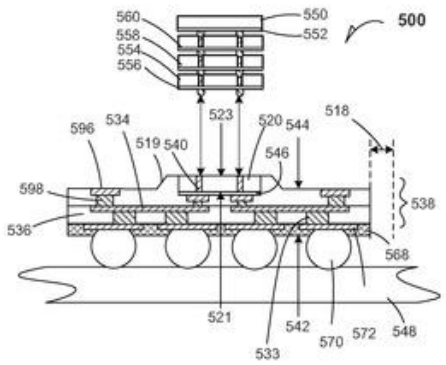
Key Player XX

Relevant Patented Technology

Use of thinner package substrates such as bumpless build-up layers in 3D integration schemes

Bumpless Build-Up Layer or BBUL is a processor packaging technology. It is bumpless since it does not use the usual tiny solder bumps to attach the silicon die to the processor package wires. It has build-up layers since it is grown or built-up around the silicon die. The usual way is to manufacture them separately and bond them together. Some semiconductor packages now use a coreless substrate, which does not include the thick resin core layer commonly found in conventional substrates.
A bumpless build-up layer (BBUL) is being formed to couple the TSV die 120 to the outside world. Although the BBUL is illustrated with the patterned first dielectric 129 and the second dielectric 136, it may be understood that several layers of metallization and dielectric can be used to form the BBUL, which ultimately is a coreless substrate with an embedded TSV die. Where the disclosed embodiments include BBUL technology on a coreless substrate, the several embodiments may be referred to as BBUL-C embodiments. Further because TSV dice are included the several embodiments may be referred to as TSV-die BBUL-C apparatus.





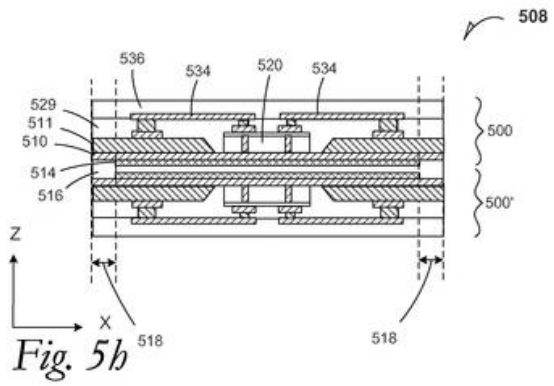
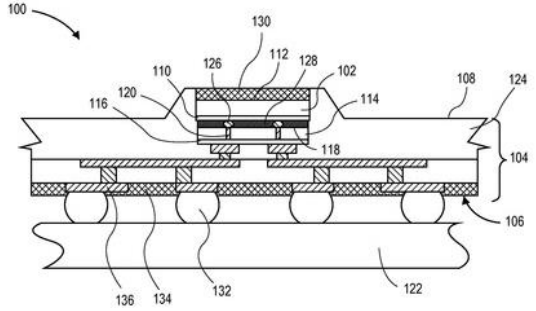
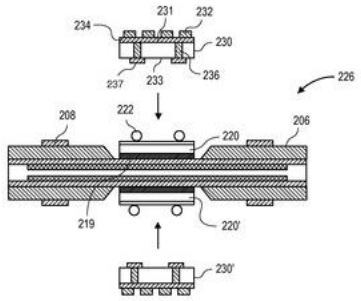
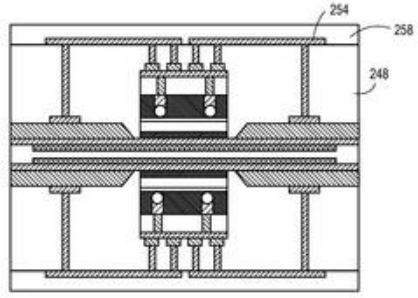


Fig. 5h







WOXXXXXXXX and WOXXXXXXX (2012)

Multi-Channel Package

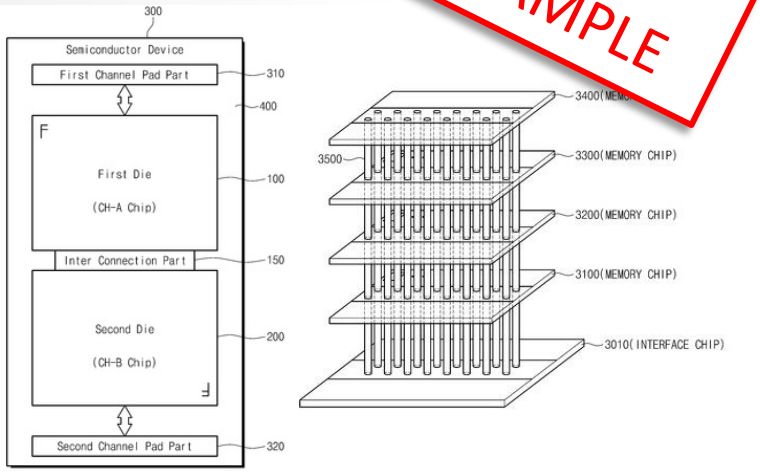
Solutions found in patents

A 2-channel semiconductor device with an 8-Gbit memory capacity may be implemented with two dies, not one die, thereby making it possible to prevent a decrease in density on a wafer and improving availability on edge dies. Similar implementations can be made with other sized memory capacity chips, such as two 16-Gbit chips combined into a 32-Gbit, 2-channel semiconductor package. As a result, an increase in production cost may be alleviated due to an increase in yield.

Each of the memory chips 3100, 3200, 3300, and 3400 is implemented with a multi-channel semiconductor device formed of two or more dies as described, thereby improving yield and reducing production cost.

The DRAM 4520 may be a DDR4 DRAM, and in one embodiment includes an interconnection part and is formed of two or more dies contained in a mono package, thereby improving yield of fabrication and making it possible to reduce production cost of the computing device.

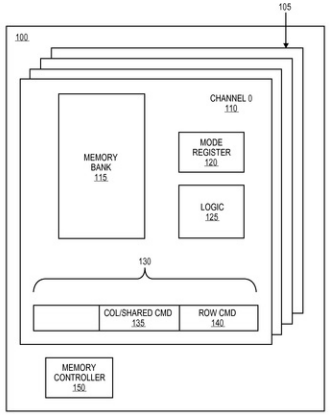
The LPDDR4 package contains four connected dies. Each physical channel has two ranks of memory connected to it. This configuration requires the design team to extend the connection in a serial direction on each of the four channels on the package. Unfortunately, a 4-die package doesn't provide 8-channel connectivity; there are only four channels of package balls on the 4-die package.



USXXXXXXX, and USXXXXXXXX (2016) Assignee XX

A memory device includes a plurality of channels 205, shown as eight channels, Channel 0 through Channel 7. In some embodiments, each channel includes a column or stack of tiles of memory strata.

The channel characteristics 300 include a requirement for an increasing number of pins for larger memory, such as the illustrated memories of density 8 Gb, 16 Gb, and 32 Gb. The division of memory into multiple channels requires command addressing at each channel, thus requiring a multiple of the pins required for a single channel of memory.



USXXXXXXXX *(2014) Assignee XX*

PATENT LITIGATIONS

ELM 3DS vs. SK Hynix

Case 1:14-cv-01432-UNA filed 21/11/2014
Plaintiff: ELM 3DS Innovation http://wyoming.intercreditreport.com/company/elm-technology-corporation-1996-000317306
Defendant: SK Hynix
Patents: US7193239, US8629542, US8653672

IN THE UNITED STATES DISTRICT COURT FOR THE DISTRICT OF DELAV
Hynix has infringed and continues to infringe the **Elm 3DS** patents,
the United States, semiconductor products with multiple stacked di
use, sell, offer for sale, and/or import into the United States, **Hynix** s
the same, with knowledge of the **Elm 3DS** patents and in the infringe

The **Elm 3DS** Patents in-suit in **ELM 3DS vs. SK Hynix** case disclose th
In one exemplary embodiment, the patents disclose a three-dimens
on top of one another and electrically connected. The disclosed te
The disclosed technology also improves memory density because m
factor requirements. Industry implementations are referred to as "
silicon vias ("TSV").

On information and belief, products sold or manufactured in the Ur
but by no means are limited to, the Apple iPhone 6, the Apple iPhor
the Samsung Galaxy Tab, and the HTC 601. These and other produc
States.

PATENT LITIGATIONS

ELM 3DS vs. Micron Technology

Case 1:14-cv-01431-UNA filed 21/11/2014
Plaintiff: ELM 3DS Innovation http://wyoming.intercreditreport.com/company/elm-technology-corporation-1996-000317306
Defendant: Micron Technology
Patents: US7193239, US7504732, US8035233, US8410617, US8629542, US8653672, US8791581, US8796862, US8824159, US8841778

IN THE UNITED STATES DISTRICT COURT FOR THE DISTRICT OF DELAWARE
Micron has infringed and continues to infringe the **Elm 3DS** Patents, direct
semiconductor products with multiple stacked die and/or electronics products
United States, **Micron** semiconductor products with multiple stacked die and/or
resulting there from.

The **ELM 3DS** Patents in-suit in **ELM 3DS vs. Micron Technology** case cover f
circuits such as memory, processors, and image sensors. These fundamental te
3DS Patents disclose technologies that enable semiconductor manufacturers to
to form interconnect circuitry for communication among the stacked die, includ

On information and belief, products sold or manufactured in the United States
Motorola Moto360, the Google Chromecast Device, the Intel Ultrabook, the
incorporating **Micron**'s infringing products are currently offered for sale in the U

Through its marketing of the infringing stacked semiconductor products, **Micro**
end users to purchase **Micron**'s stacked semiconductor products and to incorpo
markets its infringing stacked semiconductor products to third parties for inclu
DRAM products —many of which are stacked memory products—are primaril
products—many of which are stacked memory products— are primarily used in
devices. Further, **Micron** has stated that its embedded NAND Flash-based stor
computers, industrial and automotive applications, networking and other pers
through **Intel** and **Xilinx** shows that it has specifically intended to and has induce

PATENT LITIGATIONS

ELM 3DS vs. Samsung Electronics

Case 1:14-cv-01430-UNA filed 21/11/2014
Plaintiff: ELM 3DS Innovation http://wyoming.intercreditreport.com/company/elm-technology-corporation-1996-000317306
Defendant: Samsung Electronics
Patents: US7193239, US7504732, US8035233, US8410617, US8629542, US8653672, US8796862, US8824159, US8841778

IN THE UNITED STATES DISTRICT COURT FOR THE DISTRICT OF DELAWARE
Samsung has infringed and continues to infringe the **Elm 3DS** patents, di
into the United States, semiconductor products with multiple stacked die a
to use, sell, offer for sale, and/or import into the United States, **Samsun**
containing the same, with knowledge of the **Elm 3DS** patents and in the inf

The **Elm 3DS** Patents disclose three-dimensional integrated circuit structur
patents disclose a three-dimensional structure with thinned and polish
electrically connected. The disclosed technology enhances memory speed
improves memory density because multiple storage arrays can be stacked
implementations are referred to as "stacked" memories that are electricall

On information and belief, products sold or manufactured in the United St
by no means are limited to, the Apple MacBook Pro, the Dell PowerEdge
Amazon Kindle Fire HDX 7", the Microsoft Surface, and the Google Chrome
currently offered for sale in the United States.

PATENT LITIGATIONS

ELM 3DS' Patents – 1st patent family

Patent Number	Title	Priority Date	Legal Status	Expected Expiration Date	Main Claim
US8[redacted]	Adjace[redacted]antially flexible [redacted]es having integrate[redacted]ts that are bonded [redacted]r by non-pol[redacted]ayer	03/03/2003	Granted	30/12/2018	Circuitry c[redacted]ates, each substrate having integra[redacted]ach substrate having 1st substantially planar surfac[redacted]tially planar surface; 1st thermal diffusion bonds co[redacted]between a majority of 1st surfa[redacted] 2nd thermal diffusion bonds co[redacted] between a majority of 1st surface of 3rd substr[redacted]f 2nd substrate.
US7[redacted]	Thre[redacted]sional stru[redacted]mory	18/12/2003	Granted	11/04/2017	A stacked integrated circuit comp[redacted]ality of thinned substantially flexible integrated circuits, where[redacted]hinned substantially flexible integrated circuits comp[redacted]urther comprising: 1st substantially flexible in[redacted] wherein a plurality of 1st interconnections are located [redacted]lly flexible integrated circuit having 2nd surface, wherein a plu[redacted]located on 2nd surface, said 1st and 2nd surfaces face each o[redacted]nection and said plurality of 2nd interconnections are sub[redacted] and said plurality of 1st interconnections and said plurali[redacted]trically coupled together to form a plurality of vertical interco[redacted]rtical interconnections; and 3rd interconnection electrically [redacted] at least one of the plurality of thinned substantially flexibl[redacted]ntegrated circuit and the plurality of thinned substantially [redacted]itioned in a stacked relation to one another, and wherein [redacted]xible integrated circuits comprises a subs[redacted]niconductor.

PATENT LITIGATIONS

Present Status of the Cases

• In 2015, **Samsung Electronics** Co., Ltd.; **Micron Technology**, Inc.; and **SK Hynix** Inc. (collectively, "Petitioner") request **inter partes review** ("IPR") of cl… and 49 of US8907499 ("the '499 patent"): IPR2016-00708, which, on its face, is assigned to **Elm 3DS Innovations**, LLC ("Patent Owner").

*An inter partes review is used to challenge the patentability of one or more claims in a U.S. patent only on a ground that could be raised under 35 U.S.C. §§ 102 or 103, and only on the basis of prior art consisting of patents or printed publications (*http://www.uspto.gov/patents-application-process/appealing-patent-decisions/trials/inter-partes-review)

• **Patent Owner** has also asserted related US7193239; US7474004; U… US8496862; US8928119; and US8933570 in one or more of these a… US7193239 (IPR2016-00388 and IPR2016-00393); US7504732 (IPR… (IPR2016- 00394); US8653672 (IPR2016-00386); US8796862 (IPR201… (IPR2016-00691). And **Micron Technology**, Inc. and **SK Hynix** Inc. ha… 00706). **Petitioner** is also concurrently filing another **IPR petition** on …

For each of these **inter partes review**, **Dr Paul D. Franzon** submitted h…

• Before the patent trial and appeal board, **petitioners** respectfully… unpatentable, in view of the following grounds under **35 U.S.C. § 103**…

• **ELM 3DS** submitted many documents to reject these cancellations … patents filed anteriorly, publications, articles…)

Details for each **Inter Partes Review (IPR)** are described in the next slide.

To obtain more information and follow the status of the cases: https://ptabtrials.uspto.gov

PATENT LITIGATIONS

Present Status of the Inter-Partes Review (1/5)

IPR Number	Filing Date	Patent Number	Challenged Claim	Petitioner Comments Dr Paul D. Franzon	ELM 3DS Comments	Present Status
IPR2016-00708 Last Notice: 8/07	17/03/2016	US8907499 ELM 3DS	1 & 49	Petitione IPR and and 49 c on the g	ot established a any of the unpatentable. the challenged l should not be	Pending
IPR2016-00770 Last Notice: 8/07	17/03/2016	US8907499 ELM 3DS	12, 13, 24, 36, 37, 38, 53, 83, 86, 87, and 132	Petitione IPR and c 13, 24, 3 and 132 on the g	ot established a any of the 36, 37, 38, 53, entable. If the at all, it is in the challenged ous	Pending
IPR2016-00388 Last Notice: 1/07	28/12/2015	US7193239 ELM 3DS	1, 10-12, 13, 18-20, 60-63, 67, 70-73, and 77	Petitione IPR and 10-12, 1 73, anc	d a reasonable nged claims 10-3, or 77 is tion is barred as nd is redundant d by the PTO.	01/07/2 ine that there i d that Petitione ving that at least c -20, 60–63, 67, 7 allenged patent is u d has not made a f respect to the p llenged claim. The ation will be based eveloped

To obtain more information and follow the status of the cases: https://ptabtrials.uspto.gov

Excel Database

with all patents analyzed in the report with technology segmentation

This database allows multi-criteria searches and includes patent publication number, hyperlinks to the origin documents, priority date, title, abstract, patent assignees, technological segments and legal status for each member of the patent family.

KnowMade

TSV Memory Patent Landscape - September 2016

Family Number (FamPat Database)	Publication Numbers	Publication Data & Hyperlink to original document	Oldest Priority Date of the Family (YYYY-MM-DD)	Title	Abstract	Assignee	Segmentation: Claimed Invention: Package	Stacking	TSV	Bumps	Others (System, Method,...)	Current Legal Status & A
737	KR201	KR2012 A 2012-	2011-0	Semiconductor apparatus	PURPOSE: A memory device is		x					LEGAL DETAILS FOR KR20120
737	US201 US868	US2012 A1 201	2011-0	Semiconductor apparatus	Various embodiments of a		x					LEGAL DETAILS FOR US20122
737	TW20 TWI53	TW201 2012-10	2011-0	Semiconductor apparatus	Various embodiments of a		x					LEGAL DETAILS FOR TW2012
737	JP937 JP201	JP5710 JP9371	2011-0	Semiconductor device	PROBLEM TO BE SOLVED: To					x	x	LEGAL DETAILS FOR JP20121
737	US201 US937	US2012 A1 201	2011-0	Semiconductor device	Such a device is disclosed that					x	x	LEGAL DETAILS FOR US20121
730	CN105	CN1055 2016-05	2010-0	Die-Stacking Using Through-	An apparatus includes a		x		x			LEGAL DETAILS FOR CN10559
730	US934 US201	US2016 A1 2016	2014-1	Semiconductor integrated	Provided is a semiconductor			x				LEGAL DETAILS FOR US93431
730	KR201	KR2016 A 2016-	2014-1	Semiconductor integrated	The present invention			x				LEGAL DETAILS FOR KR20160
729	US201	US2016 A1 2016	2014-1	Stack semiconductor	A memory device including a stack			x				LEGAL DETAILS FOR US20161
729	KR201	KR2016 A 2016-	2014-1	Stack semiconductor	A stack semiconductor			x				LEGAL DETAILS FOR KR20160
729	US201	US2016 A1 2016	2014-1	Apparatuses and methods	Memory die can be stacked to form						x	LEGAL DETAILS FOR US20161
729	WO20	WO201 A1 2016	2014-1	Apparatuses and methods	Memory die can be stacked to form						x	LEGAL DETAILS FOR WO2016
729	TW20	TW201 2016-08	2014-1	Apparatuses and methods	The memory crystal grain may						x	LEGAL DETAILS FOR TW2016
727	CN105	CN1055 2016-04	2011-1	Self-repair logic for	The invention discloses self-				x		x	LEGAL DETAILS FOR CN10551
725	KR201	KR2016	2014-0	Semiconductor	Disclosed is a						x	LEGAL DETAILS FOR KR20160

ORDER FORM

TSV Stacked Memory – Patent Landscape Analysis

September 2016

SHIP TO
Name (Mr/Ms/Dr/Pr):
_____
Job Title:
_____
Company:
_____
Address:
_____
City:
_____
State:
_____
Postcode/Zip:
_____
Country:
_____
VAT ID Number for EU members:
_____
Tel:
_____
Email:
_____
Date:
_____

PAYMENT METHODS

Check

To pay your invoice using a check, please mail your check to the following address**:**

KnowMade S.A.R.L.
2405 route des Dolines, BP 65
06902 Valbonne Sophia Antipolis
FRANCE

Money Transfer

To pay your invoice using a bank money wire transfer please contact your bank to complete this process. Here is the information that you will need to submit the payment:

Payee: KnowMade S.A.R.L.
Bank: Banque populaire St Laurent du Var CAP 3000 - Quartier du lac- 06700 St Laurent du Var
IBAN: FR76 1560 7000 6360 6214 5695 126
BIC/SWIFT: CCBPFRPPNCE

Paypal

In order to pay your invoice via PAYPAL, you must first register at www.paypal.com. Then you can send money to the KnowMade S.A.R.L. by entering our E-mail address contact@knowmade.fr as the recipient and entering the invoice amount.

RETURN ORDER BY

E-mail: contact@knowmade.fr
Mail: KnowMade S.A.R.L. 2405 route des Dolines, 06902 Sophia Antipolis, FRANCE

PRODUCT ORDER

☐ **€4,990 – Single user license***
☐ **€5,990 – Corporate license**

For price in dollars, please use the day's exchange rate. For French customer, add 20% for VAT.

All reports are delivered electronically in pdf format at payment reception.

**Single user license means only one person at the companycan use the report. Please be aware that our publication will be watermarked on each page with the name of the recipient and of the organization (the name mentioned on the PO). This watermark will also mention that the report sharing is not allowed.*

I hereby accept Knowmade's Terms and Conditions of Sale
Signature:

Terms and Conditions of Sales

DEFINITIONS

"Acceptance": Action by which the Buyer accepts the terms and conditions of sale in their entirety. It is done by signing the purchase order which mentions "I hereby accept Knowmade's Terms and Conditions of Sale".

"Buyer": Any business user (i.e. any person acting in the course of its business activities, for its business needs) entering into the following general conditions to the exclusion of consumers acting in their personal interests.

"Contracting Parties" or "Parties": The Seller on the one hand and the Buyer on the other hand.

"Intellectual Property Rights" ("IPR") means any rights held by the Seller in its Products, including any patents, trademarks, registered models, designs, copyrights, inventions, commercial secrets and know-how, technical information, company or trading names and any other intellectual property rights or similar in any part of the world, notwithstanding the fact that they have been registered or not and including any pending registration of one of the above mentioned rights.

"License": For the reports and databases, 2 different licenses are proposed. The buyer has to choose one license:

1. One user license: a single individual at the company can use the report.
2. Multi user license: the report can be used by unlimited users within the company. Subsidiaries are not included.

"Products": Reports are established in PowerPoint and delivered on a PDF format and the database may include Excel files.

"Seller": Based in Sophia Antipolis (France headquarters), Knowmade is a technology intelligence company specialized in the research and analysis of scientific and technical information. We provide patent landscapes and scientific state of the art with high added value to businesses and research laboratories. Our intelligence digests play a key role to define your innovation and development strategy.

1. SCOPE

1.1 The Contracting Parties undertake to observe the following general conditions when agreed by the Buyer and the Seller. ANY ADDITIONAL, DIFFERENT, OR CONFLICTING TERMS AND CONDITIONS IN ANY OTHER DOCUMENTS ISSUED BY THE BUYER AT ANY TIME ARE HEREBY OBJECTED TO BY THE SELLER, SHALL BE WHOLLY INAPPLICABLE TO ANY SALE MADE HEREUNDER AND SHALL NOT BE BINDING IN ANY WAY ON THE SELLER.

1.2 This agreement becomes valid and enforceable between the Contracting Parties after clear and non-equivocal consent by any duly authorized person representing the Buyer. For these purposes, the Buyer accepts these conditions of sales when signing the purchase order which mentions "I hereby accept Knowmade's Terms and Conditions of Sale". This results in acceptance by the Buyer.

1.3 Orders are deemed to be accepted only upon written acceptance and confirmation by the Seller, within [7 days] from the date of order, to be sent either by email or to the Buyer's address. In the absence of any confirmation in writing, orders shall be deemed to have been accepted.

2. MAILING OF THE PRODUCTS

2.1 Products are sent by email to the Buyer:

- within [1] month from the order for Products already released; or
- within a reasonable time for Products ordered prior to their effective release. In this case, the Seller shall use its best endeavours to inform the Buyer of an indicative release date and the evolution of the work in progress.

2.2 Some weeks prior to the release date the Seller can propose a pre-release discount to the Buyer.

The Seller shall by no means be responsible for any delay in respect of article 2.2 above, and including in cases where a new event or access to new contradictory information would require for the analyst extra time to compute or compare the data in order to enable the Seller to deliver a high quality Products.

2.3 The mailing of the Product will occur only upon payment by the Buyer, in accordance with the conditions contained in article 3.

2.4 The mailing is operated through electronic means either by email via the sales department. If the Product's electronic delivery format is defective, the Seller undertakes to replace it at no charge to the Buyer provided that it is informed of the defective formatting within 90 days from the date of the original download or receipt of the Product.

2.5 The person receiving the Products on behalf of the Buyer shall immediately verify the quality of the Products and their conformity to the order. Any claim for apparent defects or for non-conformity shall be sent in writing to the Seller within 8 days of receipt of the Products. For this purpose, the Buyer agrees to produce sufficient evidence of such defects.

2.6 No return of Products shall be accepted without prior information to the Seller, even in case of delayed delivery. Any Product returned to the Seller without providing prior information to the Seller as required under article 2.5 shall remain at the Buyer's risk.

3. PRICE, INVOICING AND PAYMENT

3.1 Prices are given in the orders corresponding to each Product sold on a unit basis or corresponding to annual subscriptions. They are expressed to be inclusive of all taxes. The prices may be reevaluated from time to time. The effective price is deemed to be the one applicable at the time of the order.

3.2 Payments due by the Buyer shall be sent by cheque payable to Knowmade, PayPal or by electronic transfer to the following account:

Banque populaire St Laurent du Var CAP 3000 - Quartier du lac- 06700 St Laurent du Var
BIC or SWIFT code: CCBPFRPPNCE
IBAN: : FR76 1560 7000 6360 6214 5695 126

To ensure the payments, the Seller reserves the right to request down payments from the Buyer. In this case, the need of down payments will be mentioned on the order.

3.3 Payment is due by the Buyer to the Seller within 30 days from invoice date, except in the case of a particular written agreement. If the Buyer fails to pay within this time and fails to contact the Seller, the latter shall be entitled to invoice interest in arrears based on the annual rate Refi of the «BCE» + 7 points, in accordance with article L. 441-6 of the French Commercial Code. Our publications (report, database, tool...) are delivered only after reception of the payment.

3.4 In the event of termination of the contract, or of misconduct, during the contract, the Seller will have the right to invoice at the stage in progress, and to take legal action for damages.

4. LIABILITIES

4.1 The Buyer or any other individual or legal person acting on its behalf, being a business user buying the Products for its business activities, shall be solely responsible for choosing the Products and for the use and interpretations he makes of the documents it purchases, of the results he obtains, and of the advice and acts it deduces thereof.

4.2 The Seller shall only be liable for (i) direct and (ii) foreseeable pecuniary loss, caused by the Products or arising from a material breach of this agreement

4.3 In no event shall the Seller be liable for:

a) damages of any kind, including without limitation, incidental or consequential damages (including, but not limited to, damages for loss of profits, business interruption and loss of programs or information) arising out of the use of or inability to use the Seller's website or the Products, or any information provided on the website, or in the Products;

b) any claim attributable to errors, omissions or other inaccuracies in the Product or interpretations thereof.

4.4 All the information contained in the Products has been obtained from sources believed to be reliable. The Seller does not warrant the accuracy, completeness adequacy or reliability of such information, which cannot be guaranteed to be free from errors.

4.5 All the Products that the Seller sells may, upon prior notice to the Buyer from time to time be modified by or substituted with similar Products meeting the needs of the Buyer. This modification shall not lead to the liability of the Seller, provided that the Seller ensures the substituted Product is similar to the Product initially ordered.

4.6 In the case where, after inspection, it is acknowledged that the Products contain defects, the Seller undertakes to replace the defective products as far as the supplies allow and without indemnities or compensation of any kind for labor costs, delays, loss caused or any other reason. The replacement is guaranteed for a maximum of two months starting from the delivery date. Any replacement is excluded for any event as set out in article 5 below.

4.7 The deadlines that the Seller is asked to state for the mailing of the Products are given for information only and are not guaranteed. If such deadlines are not met, it shall not lead to any damages or cancellation of the orders, except for non-acceptable delays exceeding [4] months from the stated deadline, without information from the Seller. In such case only, the Buyer shall be entitled to ask for a reimbursement of its first down payment to the exclusion of any further damages.

4.8 The Seller does not make any warranties, express or implied, including, without limitation, those of saleability and fitness for a particular purpose, with respect to the Products. Although the Seller shall take reasonable steps to screen Products for infection of viruses, worms, Trojan horses or other codes containing contaminating or destructive properties before making the Products available, the Seller cannot guarantee that any Product will be free from infection.

5. FORCE MAJEURE

The Seller shall not be liable for any delay in performance directly or indirectly caused by or resulting from acts of nature, fire, flood, accident, riot, war, government intervention, embargoes, strikes, labor difficulties, equipment failure, late deliveries by suppliers or other difficulties which are beyond the control, and not the fault of the Seller.

6. PROTECTION OF THE SELLER'S IPR

6.1 All the IPR attached to the Products are and remain the property of the Seller and are protected under French and international copyright law and conventions.

6.2 The Buyer agreed not to disclose, copy, reproduce, redistribute, resell or publish the Product, or any part of it to any other party other than employees of its company. The Buyer shall have the right to use the Products solely for its own internal information purposes. In particular, the Buyer shall therefore not use the Product for purposes such as:

- Information storage and retrieval systems;
- Recordings and re-transmittals over any network (including any local area network);
- use in any timesharing, service bureau, bulletin board or similar arrangement or public display;
- Posting any Product to any other online service (including bulletin boards or the Internet);
- Licensing, leasing, selling, offering for sale or assigning the Product.

6.3 The Buyer shall be solely responsible towards the Seller of all infringements of this obligation, whether this infringement comes from its employees or any person to whom the Buyer has sent the Products and shall personally take care of any related proceedings, and the Buyer shall bear related financial consequences in their entirety.

6.4 The Buyer shall define within its company point of contact for the needs of the contract. This person will be the recipient of each new report in PDF format. This person shall also be responsible for respect of the copyrights and will guaranty that the Products are not disseminated out of the company.

7. TERMINATION

7.1 If the Buyer cancels the order in whole or in part or postpones the date of mailing, the Buyer shall indemnify the Seller for the entire costs that have been incurred as at the date of notification by the Buyer of such delay or cancellation. This may also apply for any other direct or indirect consequential loss that may be borne by the Seller, following this decision.

7.2 In the event of breach by one Party under these conditions or the order, the non-breaching Party may send a notification to the other by recorded delivery letter upon which, after a period of thirty (30) days without solving the problem, the non-breaching Party shall be entitled to terminate all the pending orders, without being liable for any compensation.

8. MISCELLANEOUS

All the provisions of these Terms and Conditions are for the benefit of the Seller itself, but also for its licensors, employees and agents. Each of them is entitled to assert and enforce those provisions against the Buyer.

Any notices under these Terms and Conditions shall be given in writing. They shall be effective upon receipt by the other Party.

The Seller may, from time to time, update these Terms and Conditions and the Buyer, is deemed to have accepted the latest version of these terms and conditions, provided they have been communicated to him in due time.

9. GOVERNING LAW AND JURISDICTION

9.1 Any dispute arising out or linked to these Terms and Conditions or to any contract (orders) entered into in application of these Terms and Conditions shall be settled by the French Commercial Courts of Grasse, which shall have exclusive jurisdiction upon such issues.

9.2 French law shall govern the relation between the Buyer and the Seller, in accordance with these Terms and Conditions.

KnowMade SARL
2405 route des Dolines
06902 Sophia Antipolis, France

www.knowmade.com
contact@knowmade.fr