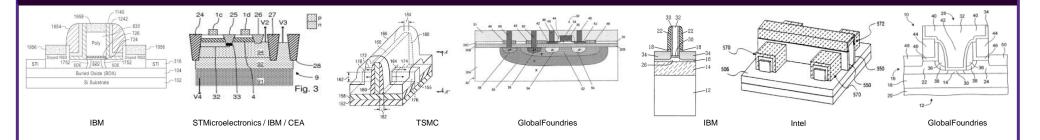
### **FD-SOI Patent Landscape** *Fully Depleted Transistors on SOI Substrate*

REPORT

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**Technological Segmentation** 

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Process level: transistor, device and circuit.

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#### II. Patent Landscape

For each architecture (planar FD-SOI and SOI FinFET):

- Time Evolution of Patent Publications
- Countries of Patent Filings
- Time Evolution by Country of Patent Filing
- Main Patent Assignees Ranking
- Main Joint Developments and Collaborations
- Time Evolution of Patent Assignees
- Countries of Patent Filings for Main Patent Assignees
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strength/weakness, key patents.										

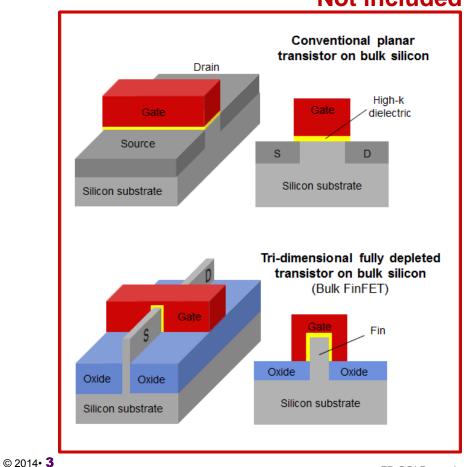
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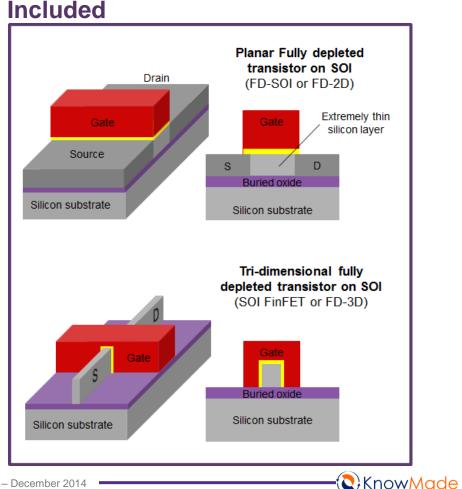
REPORTI

# **Scope of the Report**

- REPORT ' This report provides a detailed picture of the patent landscape for Fully Depleted Transistors on . on-Insulator Substrate (planar FD-SOI and SOI FinFET).
- This report does not include patents related to fully depleted transistor on bulk substrate (Bulk FinFET). • This report does not include patents related to SOI wafer.



#### Not included



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### **Rationales for Choice**

REPORT / SAMPLE

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#### Recently we observe significant moves in the arena suggesting there is a place for FD-SOI in the market.

- Samsung and STMicroelectronics signed a strategic agreement in May 2014 to expand 28nm FD-SOI technology. Samsung is licensing 28nm FD-SOI. Synopsys, STMicroelectronics and Samsung collaborate to accelerate adoption of 28nm FD-SOI technology for SoC design.
- **GlobalFoundries**, a foundry for 28nm FD-SOI, plans to field a 14nm FD-SOI process after 2015. Manfred Horstmann, Director of Products & Integration for GlobalFoundries in Dresden said at Semicon Europe 2014 that FD-SOI would be their focus for the next few years. They think it's the right solution for SOCs.
- STMicroelectronics describes the FD-SOI as scalable with roadmap down to 10nm, with 14nm node in development. For STMicroelectronics, FD-SOI is very well suited for cost-sensitive markets requiring power efficiency and performance. At Semicon Europe 2014, they described FD-SOI applications such as mobile, consumer, network infrastructure and automotive. FD-SOI extends the lifetime of 28nm offering outstanding efficiency at all levels. STMicroelectronics called it FDSOI with UTBB structure (Ultra Thin Body and BOX SOI), also called UTSOI.
- **CEA-Leti**'s work on FDSOI-UTBB Technology has contributed to demonstrate that such technology meets the requirement for mobile SoC.
- **IBM** describes FDSOI (called also ETSOI) as a promising option for high performance and SoC applications that can be scaled beyond 20nm node dimensions.
- **Soitec** breakthrough in making the ultrathin SOI wafers with ultrathin box made industrialization reality. Soitec and Shin-Etsu Handotai announce Smart Cut licensing extension and expanding technology cooperation in 2012. Sun Edison is also a FDSOI substrate supplier.
- Low Power Electronics Association & Project (aka LEAP) and Renesas Electronics see lots of possibilities with FD-SOI, which they call SOTB (for silicon-on-thin-box).
- According to VeriSilicon's figures from the recent Shanghai FD-SOI forum, at 28nm, FD-SOI savings are of 19% in area, 71% in standby power and 58% in power over bulk.
- Handel Jones, CEO from International Business Strategies is convinced that FD-SOI is the best technology for IoT applications, mainly because of memory driving cost, size and power consumption requirements. He sees FD-SOI offering lower power, lower cost/gate, re-usable IP and scalability to 14nm.

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### **Key Features of the Report**

- REPORT The report provides essential patent data for FD-SOI including both planar and 3D (finFET) architectures
- It identifies more than **30 patent holders** of **FD-SOI** related intellectual property. It provides in-depth analysis key technology segments and key players including:
  - Time evolution of patent publications and countries of patent filings.
  - Current legal status of patents.
  - Ranking of main patent applicants.
  - Joint developments and IP collaboration network of main patent applicants.
  - Segmentation by architecture (planar FD-SOI, SOI FinFET) and process level (transistor, device, circuit).
  - Key patents.
  - Granted patents near expiration.
  - Relative strength of main companies IP portfolio.
  - Matrix applicants / technology segments for more than 20 companies.
- The "FD-SOI IP" profiles of 10 major companies is presented, with key patents, patented technologies, • partnerships, and IP strength and strategy.
- The report also provides an extensive **Excel database** with all patents analyzed in the report with technology • segmentation. This database allows multi-criteria searches: patent publication number, hyperlinks to the original documents, priority date, title, abstract, claims, patent assignees, technological segments, legal status for each member of the patent family.
- This report does not provide any insight analyses or counsel regarding legal aspects or the validity of any • individual patent. Knowmade is research firm that provide patent and technical analysis and opinions. The research, technical analysis and/or work contained herein is not a legal opinion and should not be construed as such.

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# Methodology (1/2)

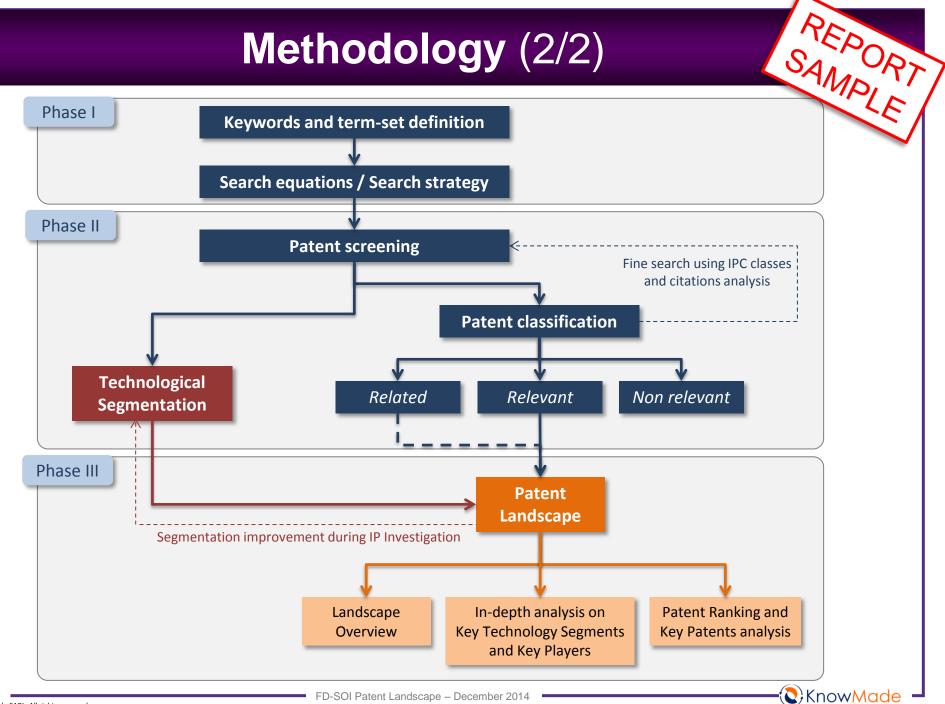
- REPORT • The data were extracted from the FamPat worldwide patent database (Questel-ORBIT) which provides by million patent documents from 95 offices.
- The patents search was performed in October 2014, hence patents published after this date will not be available in this report.
- The patent selection is done both **automatically and manually** (search strategy detailed in next slides).

748 patent families have been selected for the Fully Depleted Transistor Patent Landscape

- The statistical analysis was performed with Questel IP Business Intelligence software.
- The patents were **manually categorized** using keyword analysis of patent title, abstract and claims, in conjunction with expert review of the subject-matter of inventions (details in next slides).
- The patents were organized according to **FamPat's family rules** (variation of EPO strict family): A Patent Family comprises patents linked by exactly same priority numbers (strict family), plus comparison of priority and application numbers, specific rules by country and information gathered from other sources (national files, legal status ...).

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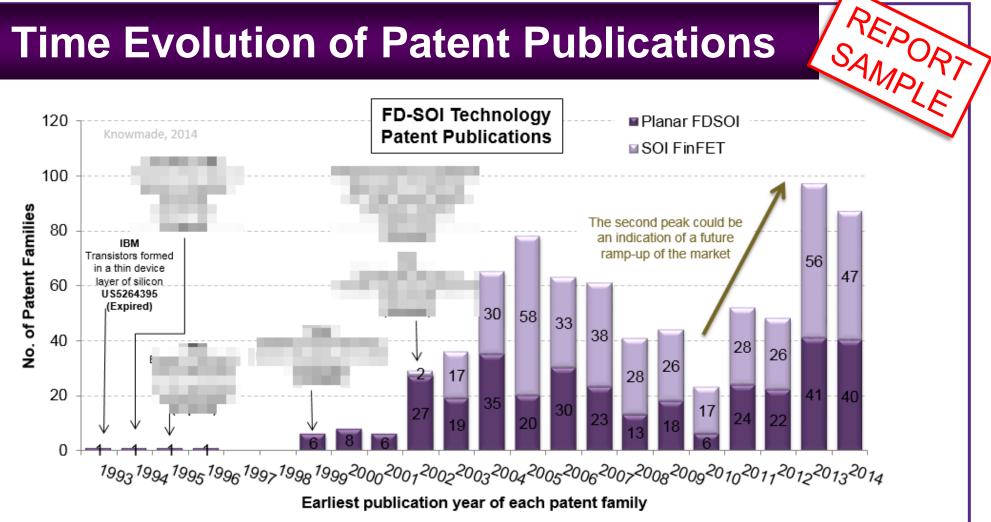
# Methodology (2/2)



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# **Time Evolution of Patent Publications**

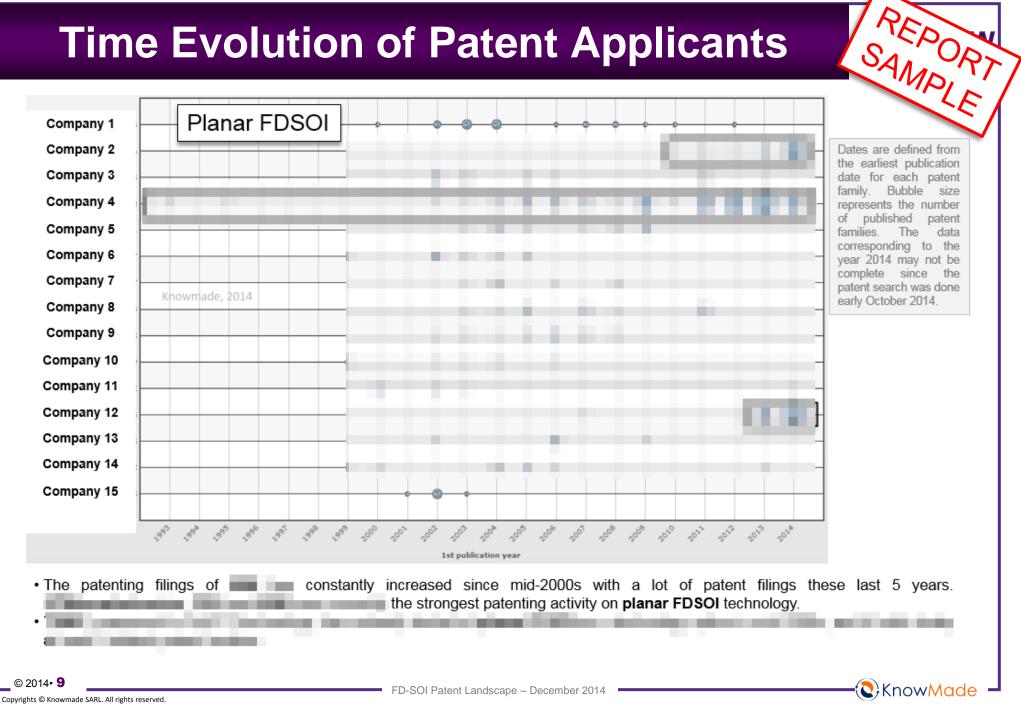


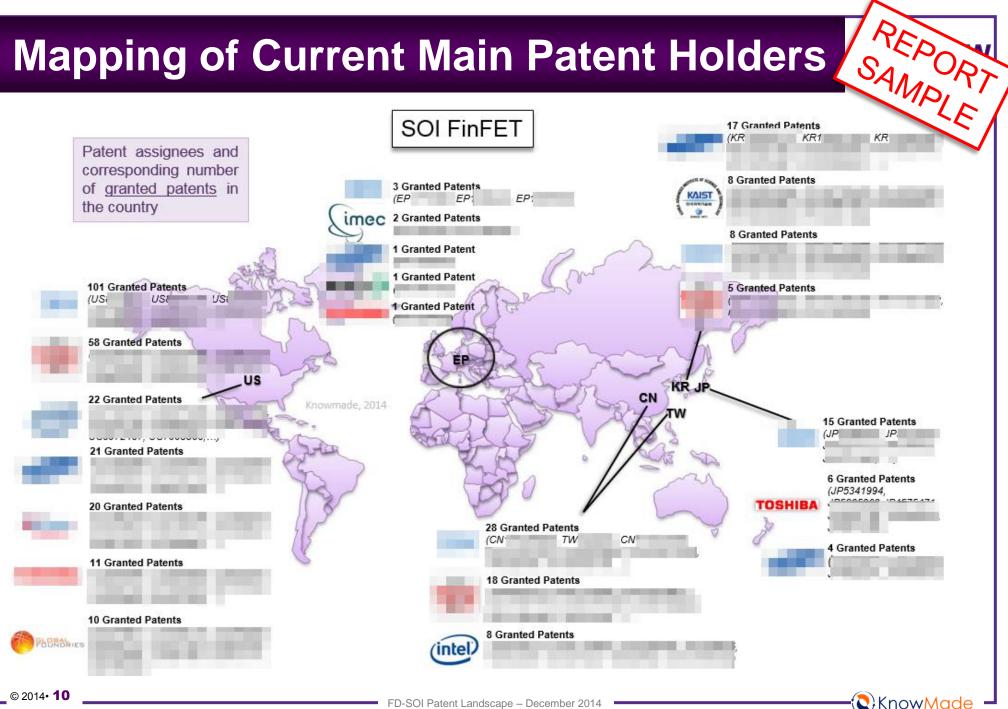
Note: The data corresponding to the year 2014 are not complete since the patent search was done in early October 2014.

- Early-1990s, IBM published first patents describing transistors grown on SOI (USXXXXXXX and JPXXXXXXX). Since then, at least 300 relevant patent families describing planar FDSOI technology have been published. The patents related to the SOI FinFET technology appeared in the beginning-2000s, with at least 400 patent families today.
- The number of new patent applications is increasing and we observe a second peak of patent publications. This could be an indication of a growth of the market in the next few years.

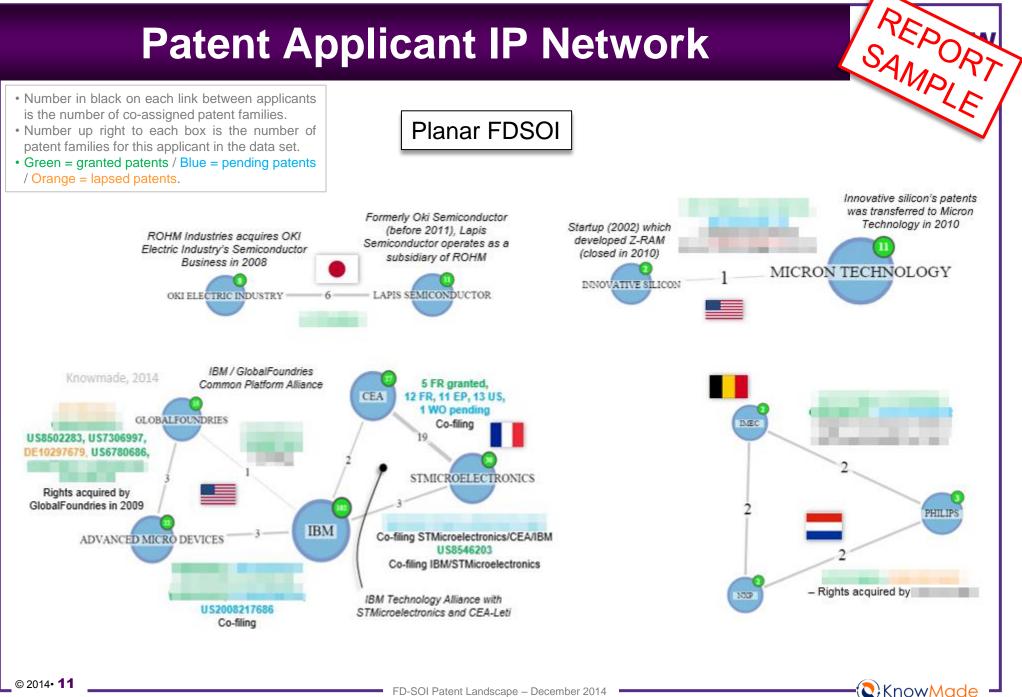
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### **Time Evolution of Patent Applicants**





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# Summary of Applicant's Patent Portfolio

SOI FinFET

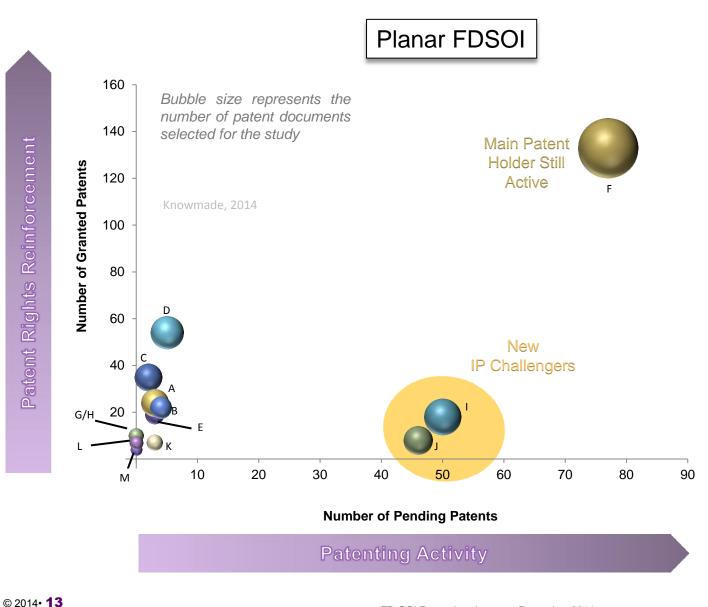
Patent Applicants	No. of patent families	Oldest priority date of the patent portfolio	No. of patent families filed / yr	No. of patents documents	No. of patents / Patent family	Patents average age	% granted	% pending	lapsed,	No. of alive patents / family	No. (		ed pate ly count	nt docume try	ents
		portiono	(average)		(average)	(Y)			expired)	(granted, pending)	US	EP	JP	CN/TW/ HK	KR
Company 1															
Company 2															
Company 3							100	100							
Company 4			1.00	10.0					100						
Company 5															
Company 6						1.1	100	100	100						
Company 7															
Company 8		1000							100						
Company 9			1.00	10.0			100		1000						
Company 10				12.1					100						
Company 11	8	04/09/2001	0.6	10	1	8	90%	0%	10%	1.1	1				8
Company 12	8	06/02/2006	0.9	20	3	3	30%	60%	10%	2.3	4		1		
Company 13	7	07/10/2003	0.6	10	1	2	60%	40%	0%	1.4	6				
Company 14	7	22/11/2002	0.6	26	4	7	65%	27%	8%	3.4	6	1	1	4	

: highest value in column

: lowest value in column

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### **Leadership of Patent Applicants**



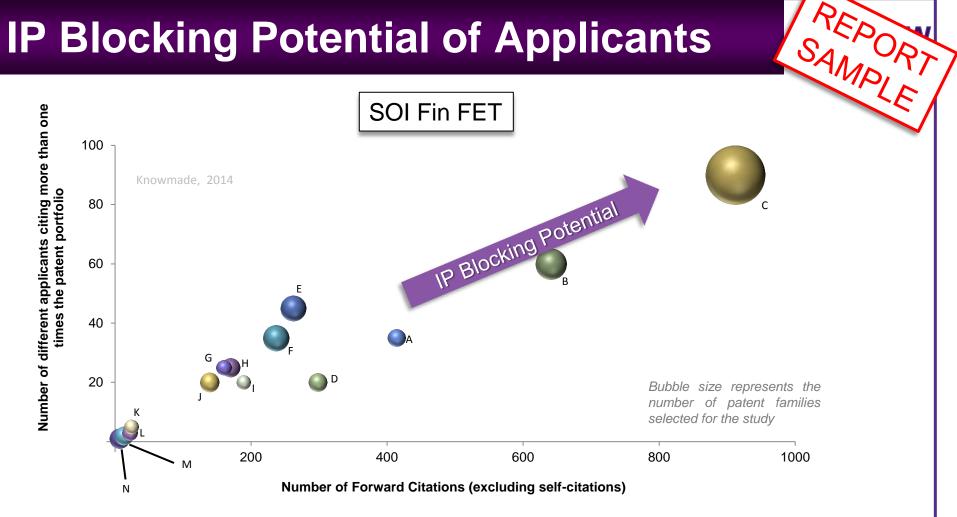
 Company F is leading the FDSOI patent landscape with a strong enforceable patent portfolio (130+ granted patent mainly in USA) and an important patenting activity (70+ pending patents), suggesting that significant number of granted patents could be expected in the coming years.

REPORT

- Companies I and J are becoming major forces in the FDSOI patent landscape with about 50 pending patents filed these last 2 years. Note they focus their FDSOI IP mainly on XXXXX.
- Companies C and D have significant enforceable patents (35 and 54 granted patents respectively, mainly in XXXX), but they have been less active since mid-2000s.

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# **IP Blocking Potential of Applicants**



The more the number of forward citations from different patent applicants is high, the more the capacity to hamper the other firms' attempts to patent a related invention is important.

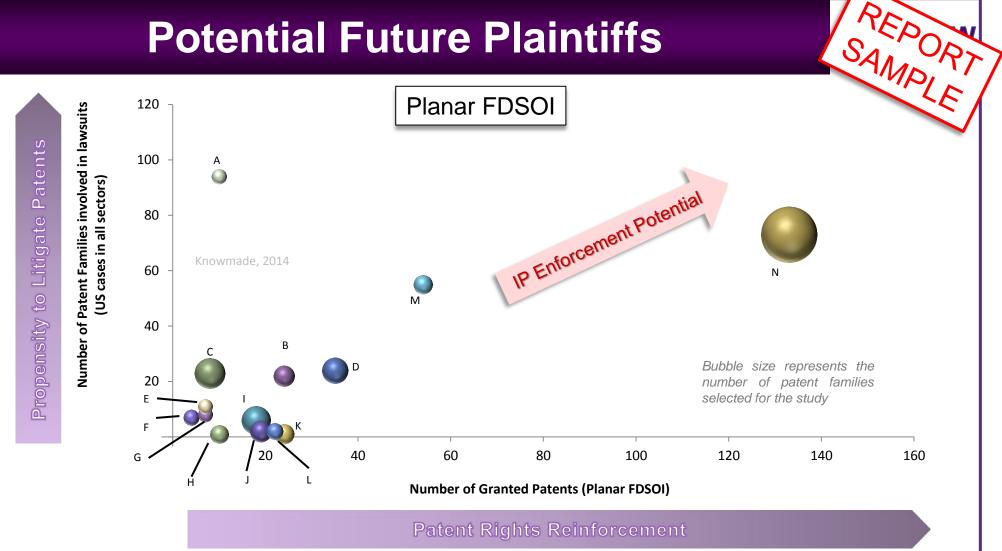
- Company C has the most important IP blocking potential in SOI FinFET area. Its patent portfolio received more than 900 forward citations from at least 90 different patent applicants.
- Company B has a significant IP blocking potential ahead of Companies A, E, F and D.
- Note, however, that the identification of a "blocking patent" requires an in-depth specific analysis of each patent documents.

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FD-SOI Patent Landscape – December 2014

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### **Potential Future Plaintiffs**

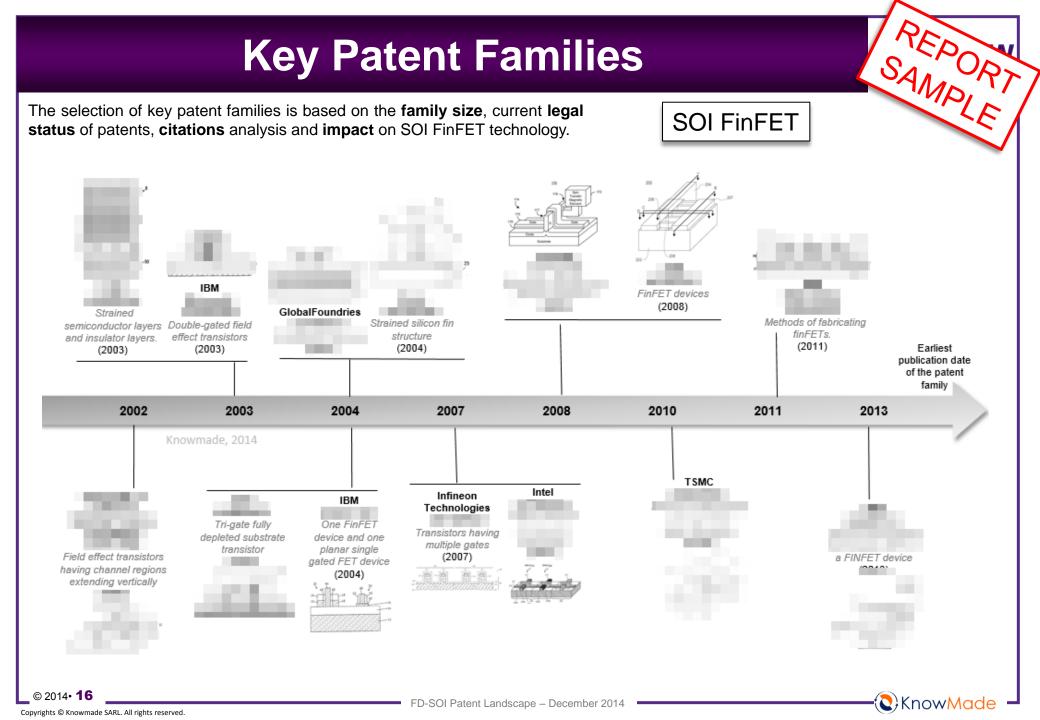


- Company N has the most significant IP enforcement potential in FDSOI area. It holds an important number of enforceable patents (granted) on planar FDSOI and has a significant propensity to litigate its patents (according to the number of US cases in all industrial sectors).
- Companies A and M have noticeable IP enforcement potential in FDSOI area. Company M combines a significant number of granted patents with a noticeable number of US lawsuits in all fields. Company A has few number of granted patents on planar FDSOI but, according to the number of US cases in all sectors, it shows an important propensity to assert its patent rights. © 2014•15

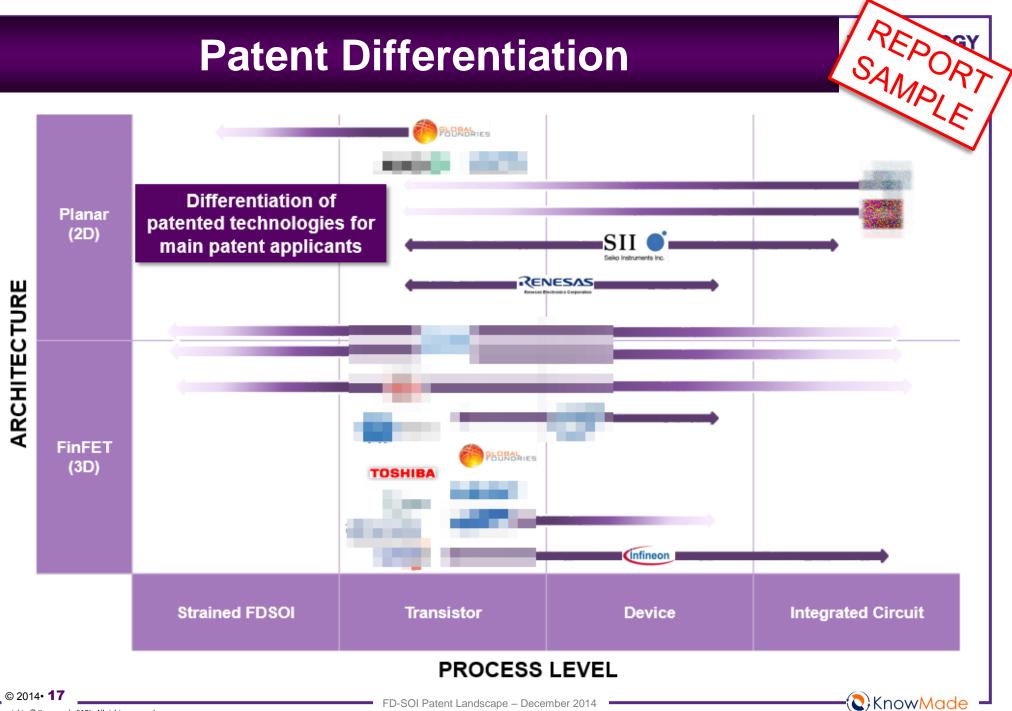
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FD-SOI Patent Landscape – December 2014

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### **Patent Differentiation**



### **GlobalFoundries/AMD: Last News**

- 2014: Acquisition of IBM's chip-manufacturing unit. GlobalFoundries acquire wafer fabs; IBM's commercial microelectronics business, which includes ASIC and foundry; over 10,000 IBM patents related to semiconductor manufacturing; and over 5000 fab and ASIC employees. GlobalFoundries will supply all IBM's 22nm, 14nm and 10nm ICs for the next 10 years.
- 2014: GlobalFoundries licensed Samsung's 14nm FinFET process technology. AMD gains access to a capable 14-nm FinFET tech for the production of its future CPUs and SOCs. AMD's Kaveri APUs actually ran slower than their predecessors after transitioning from GlobalFoundries's 32-nm SOI process to 28-nm bulk silicon.
- 2014: GlobalFoundries will supply all IBM's 22nm, 14nm and 10nm ICs for the next 10 years.
- 2013: AMD has made two new 32nm SOI-based product announcements.
- 2012: STMicroelectronics signed an agreement with GlobalFoundries for both 28nm and 20nm FD-SOI production. ("20nm" changed then to "14nm").
- 2012: AMD sheds its stake in GlobalFoundries.
- 2010: Acquisition of Chartered Semiconductor.
- 2009: Creation of GlobalFoundries by the divestiture of the manufacturing arm of Advanced Micro Devices (AMD).

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# **GlobalFoundries/AMD: Tech. Choice**

- GlobalFoundries is the world's second largest foundry behind TSMC.
- Technology choices of GlobalFoundries are not obvious. According all collaborations and announcements, we can suggest that:
  - At 28nm they seem to develop 28HPP high power performance and

28SLP super low power, that is **bulk planar 28nm processes**.

-They also develop **28nm Planar FDSOI** with STMicroelectronics.

- GlobalFoundries is gate-first HKMG (High-K Metal Gate).



REPORT

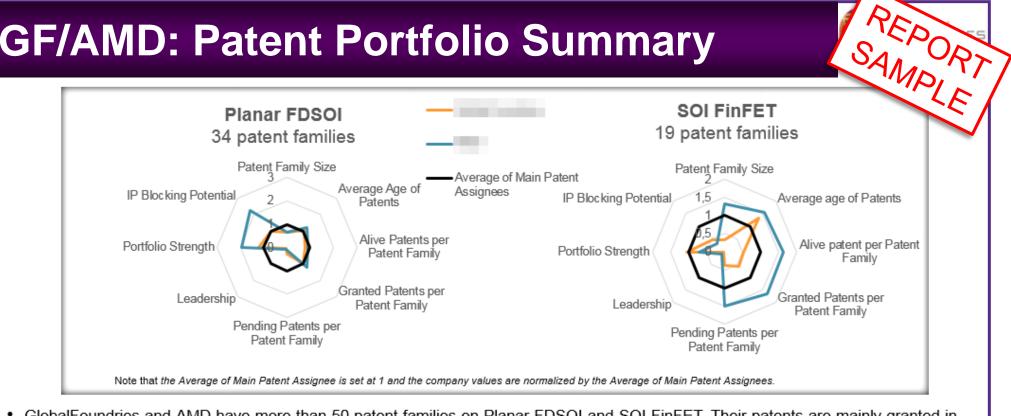
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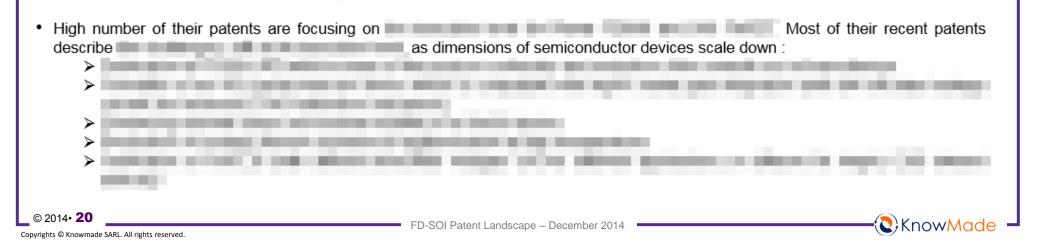
Source: GlobalFoundries

- At 20nm GlobalFoundries works on a bulk planar process 20LPM in collaboration with IBM. They plan to field a 20nm FDSOI process in 2015, according to Mike Mendicino, senior director of product management at the silicon foundry provider.
- At 14nm GlobalFoundries has licensed Samsung's FinFET on bulk technology so they confirm that <u>they give up on their 14XM</u> <u>process</u>. The firm says Samsung's process tech has two key advantages over 14XM. Samsung's tech is further along in development, so the schedule is more attractive, and **Samsung's 14nm FinFET (on bulk)** tech provides better area scaling by cramming more gates into a given area. The two companies will offer capacity from GlobalFoundries Fab 8 and Samsung fabs S1, S2 and S3. They will also develop **14nm FinFET on SOI** in collaboration with IBM and **14nm FDSOI** with STMicroelectronics.
- At 10nm, IBM, GlobalFoundries, and Samsung along, with STMicroelectronics and UMC, have described a 10nm logic process with the tightest contacted poly pitch (64nm) and metallization pitch (48nm) ever reported in FinFETs on both bulk and SOI substrates at the VLSI conference in June 2014.

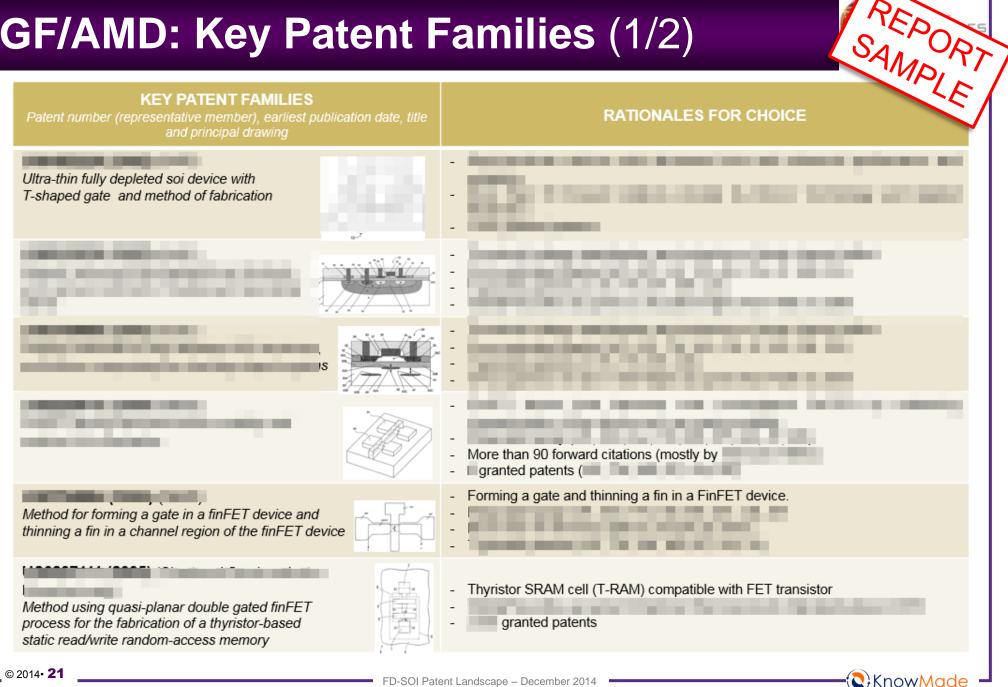
# **GF/AMD:** Patent Portfolio Summary



GlobalFoundries and AMD have more than 50 patent families on Planar FDSOI and SOI FinFET. Their patents are mainly granted in ٠



# **GF/AMD: Key Patent Families** (1/2)



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### **Excel Database**

#### with all patents analyzed in the report with technology segmentation



This database allows multi-criteria searches and includes patent publication number, hyperlinks to the original documents, priority date, title, abstract, patent assignees, technological segments and legal status for each member of the patent family.

REPORT I SAMPLE

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-SOI Pate	ent Landscape	- December	2014		SOI ecture		FD-SOI Process Level					
n <b>ily Number</b> (FamPat Database) <mark>-</mark>	Patent Numbers	Hyperlink to original documents	Oldest Priority Date of the Family (YYYY-MM-DD)	Title 🗸	Abstract	Assignee	Planar FD-SOI	SOI FinFET	Strained FD-SOI	Transistor 🗸	Device 👻	Circui
19657	FR30(===	FR30	2013-03-22	INTEGRATED	Questel	ST	x					х
19282	FR30(	FR30	2013-03-28	PROCESS OF	A method for	ST	X					х
19282	US20:	US20	2013-03-28	Method for	A method for	ST	x					х
19282	EP27	EP27	2013-03-28	A method of	The method	ST	X					x
80022	FR30(	FR30	2013-03-21	PROCESS OF	Questel	ST	X		x			
80022	EP278	EP27	2013-03-21	Method for	The method	ST	x		x			
43806	US20	US20	2013-03-14	Back-gated	A method of	IBM	x			x		
37655	US20:	US20	2013-03-13	Hybrid ETSOI	In one aspect,	IBM	х			x		
37655	US20	US20	2013-03-13	Hybrid ETSOI	In one aspect,	IBM	X			x		
72748	US20:	US20	2013-03-08	Extremely	A method of	\$44(jan)	X				x	
72748	US20:	US20	2013-03-08	Extremely	A method of	18.54	X				х	
91426	WO2	WO2	2013-02-28	Low leakage	The invention	MAR AND	x		[[		x	x
89562	W02	WO2	2013-02-28	Dual sti	The invention	the local	X					X
75713	US20:	US20	2012-01-05	Integrated	A structure	844	x		Ű.			Х
84219	IN201 =	IN37	2013-12-03	Fdsoi-	Present	CHOMADE.	x				x	
72963	WO2(	W02	2012-07-28	Improved	The structures,	10.0	x			x		
11403	US20:	US20	2011-03-21	Fin field-	A fin field-	ALC: NO		x		x		
11403	US20:	US20	2011-03-21	Fin field-	A fin field-	1000		x		x		
54420	US20:	US20	2011-03-15	High density	Dual	19.8.2		x				X
54422	US20	US20	2011-03-14	Fin fet	A FinFET	1984		х			х	
7820	CN10	CN1	2011-02-25	Manufacturi	The invention	NOT 10,403 (00)		х		x		
42166	US20	US20	2011-01-31	Method for	A method for	1010		x		x		
47201	TW20	TW2	2011-01-31	Method for	A method for	une to be		x		x		
37401	WO2	WO2	2011-01-27	Finfet	A	AND IN .		x			х	
37401	CN10	CN1	2011-01-27	Finfet	A	en/		х			х	
37401	US201	US2	2011-01-27	FINFET	۵	(高品)		x	2		X	

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December 2014

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	For French customer, add 20% for VAT.							
	All reports are delivered electronically in pdf format at							
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	the organization (the name mentioned on the PO). This watermark will also mention that the report sharing is not allowed.							
	win also menuon una une report sharing is not anowed.							
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The Seller shall by no means be responsible for any delay in respect of article 2.2 above, and including in cases where a new event or access to new contradictory information would require for the analyst extra time to compute or compare the data in order to enable the Seller to deliver a high quality Products.

2.3 The mailing of the Product will occur only upon payment by the Buyer, in accordance with the conditions contained in article 3.

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BIC or SWIFT code: CCBPFRPPNCE

#### IBAN: : FR76 1560 7000 6360 6214 5695 126

To ensure the payments, the Seller reserves the right to request down payments from the Buyer. In this case, the need of down payments will be mentioned on the order.

3.3 Payment is due by the Buyer to the Seller within 30 days from invoice date, except in the case of a particular written agreement. If the Buyer fails to pay within this time and fails to contact the Seller, the latter shall be entitled to invoice interest in arrears based on the annual rate Refi of the «BCE» + 7 points, in accordance with article L. 441-6 of the French Commercial Code. Our publications (report, database, tool...) are delivered only after reception of the payment.

3.4 In the event of termination of the contract, or of misconduct, during the contract, the Seller will have the right to invoice at the stage in progress, and to take legal action for damages.

#### 4. Liabilities

4.1 The Buyer or any other individual or legal person acting on its behalf, being a business user buying the Products for its business activities, shall be solely responsible for choosing the Products and for the use and interpretations he makes of the documents it purchases, of the results he obtains, and of the advice and acts it deduces thereof.

4.2 The Seller shall only be liable for (i) direct and (ii) foreseeable pecuniary loss, caused by the Products or arising from a material breach of this agreement

4.3 In no event shall the Seller be liable for:

a) damages of any kind, including without limitation, incidental or consequential damages (including, but not limited to, damages for loss of profits, business interruption and loss of programs or information) arising out of the use of or inability to use the Seller's website or the Products, or any information provided on the website, or in the Products;

b) any claim attributable to errors, omissions or other inaccuracies in the Product or interpretations thereof.

4.4 All the information contained in the Products has been obtained from sources believed to be reliable. The Seller does not warrant the accuracy, completeness adequacy or reliability of such information, which cannot be guaranteed to be free from errors.

4.5 All the Products that the Seller sells may, upon prior notice to the Buyer from time to time be modified by or substituted with similar Products meeting the needs of the Buyer. This modification shall not lead to the liability of the Seller, provided that the Seller ensures the substituted Product is similar to the Product initially ordered.

4.6 In the case where, after inspection, it is acknowledged that the Products contain defects, the Seller undertakes to replace the defective products as far as the supplies allow and without indemnities or compensation of any kind for labor costs, delays, loss caused or any other reason. The replacement is guaranteed for a maximum of two months starting from the delivery date. Any replacement is excluded for any event as set out in article 5 below.

4.7 The deadlines that the Seller is asked to state for the mailing of the Products are given for information only and are not guaranteed. If such deadlines are not met, it shall not lead to any damages or cancellation of the orders, except for non-acceptable delays exceeding [4] months from the stated deadline, without information from the Seller. In such case only, the Buyer shall be entitled to ask for a reimbursement of its first down payment to the exclusion of any further damages.

4.8 The Seller does not make any warranties, express or implied, including, without limitation, those of saleability and fitness for a particular purpose, with respect to the Products. Although the Seller shall take reasonable steps to screen Products for infection of viruses, worms, Trojan horses or other codes containing contaminating or destructive properties before making the Products available, the Seller cannot guarantee that any Product will be free from infection.

#### 5. Force majeure

The Seller shall not be liable for any delay in performance directly or indirectly caused by or resulting from acts of nature, fire, flood, accident, riot, war, government intervention, embargoes, strikes, labor difficulties, equipment failure, late deliveries by suppliers or other difficulties which are beyond the control, and not the fault of the Seller.

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### **Terms and Conditions of Sales**

#### 6. Protection of the Seller's IPR

6.1 All the IPR attached to the Products are and remain the property of the Seller and are protected under French and international copyright law and conventions.

6.2 The Buyer agreed not to disclose, copy, reproduce, redistribute, resell or publish the Product, or any part of it to any other party other than employees of its company. The Buyer shall have the right to use the Product solely for its own internal information purposes. In particular, the Buyer shall therefore not use the Product for purposes such as:

- Information storage and retrieval systems;
- Recordings and re-transmittals over any network (including any local area network);
- use in any timesharing, service bureau, bulletin board or similar arrangement or public display;
- Posting any Product to any other online service (including bulletin boards or the Internet);
- Licensing, leasing, selling, offering for sale or assigning the Product.

6.3 The Buyer shall be solely responsible towards the Seller of all infringements of this obligation, whether this infringement comes from its employees or any person to whom the Buyer has sent the Products and shall personally take care of any related proceedings, and the Buyer shall bear related financial consequences in their entirety.

6.4 The Buyer shall define within its company point of contact for the needs of the contract. This person will be the recipient of each new report in PDF format. This person shall also be responsible for respect of the copyrights and will guaranty that the Products are not disseminated out of the company.

#### 7. Termination

7.1 If the Buyer cancels the order in whole or in part or postpones the date of mailing, the Buyer shall indemnify the Seller for the entire costs that have been incurred as at the date of notification by the Buyer of such delay or cancellation. This may also apply for any other direct or indirect consequential loss that may be borne by the Seller, following this decision.

7.2 In the event of breach by one Party under these conditions or the order, the non-breaching Party may send a notification to the other by recorded delivery letter upon which, after a period of thirty (30) days without solving the problem, the non-breaching Party shall be entitled to terminate all the pending orders, without being liable for any compensation.

#### 8. Miscellaneous

All the provisions of these Terms and Conditions are for the benefit of the Seller itself, but also for its licensors, employees and agents. Each of them is entitled to assert and enforce those provisions against the Buyer.

Any notices under these Terms and Conditions shall be given in writing. They shall be effective upon receipt by the other Party.

The Seller may, from time to time, update these Terms and Conditions and the Buyer, is deemed to have accepted the latest version of these terms and conditions, provided they have been communicated to him in due time.

#### 9. Governing law and jurisdiction

9.1 Any dispute arising out or linked to these Terms and Conditions or to any contract (orders) entered into in application of these Terms and Conditions shall be settled by the French Commercial Courts of Grasse, which shall have exclusive jurisdiction upon such issues.

9.2 French law shall govern the relation between the Buyer and the Seller, in accordance with these Terms and Conditions.

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