

# FD-SOI Patent Landscape

## Fully Depleted Transistors on SOI Substrate

The major proponents of the FD-SOI technology have strong IP arms, but other unexpected players known as not supporting FDSOI are also present

### REPORT OUTLINE

- FD-SOI.
- Patent Landscape.
- December 2014.
- PDF & Excel file.
- €3,990 (corporate license).

### KEY FEATURES OF THE REPORT

The report provides **essential patent data** for FD-SOI including:

- Time evolution of patent publications and countries of patent filings.
- Current legal status of patents.
- Ranking of main patent applicants.
- Joint developments and IP collaboration network of main patent applicants.
- Segmentation by architecture (planar FD-SOI, SOI FinFET) and process level (transistor, device, circuit).
- Key patents.
- Granted patents near expiration.
- Relative strength of main companies IP portfolio.
- Matrix applicants / technology segments.
- FD-SOI IP profiles of major companies with key patents, patented technologies, partnerships, and IP strength and strategy.

The report also provides an extensive **Excel database** with all patents analyzed in the study.

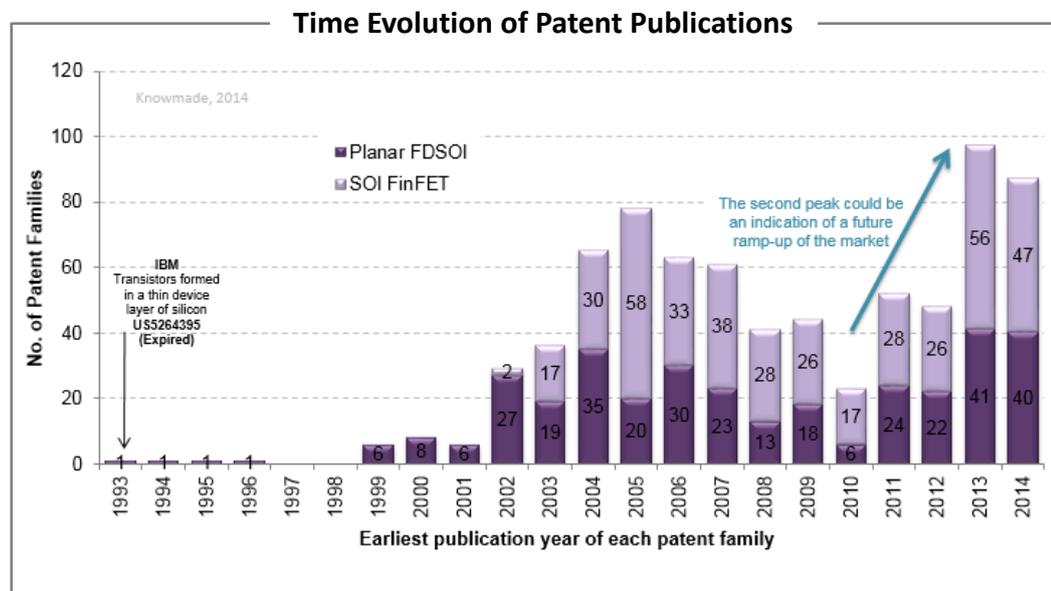
### OBJECTIVE OF THE REPORT

- Provide an overview of FD-SOI technology.
- Review context for FD-SOI technology.
- Understand the patent landscape for FD-SOI.
- Identify key patents of FD-SOI technology.
- Understand trends in FD-SOI IP.
- Identify the major players in FD-SOI IP and the relative strength of their patent portfolio.
- Identify new players in FD-SOI IP.
- Identify IP collaboration networks between key players.

### DESCRIBING THE IP SITUATION OF FD-SOI ARENA

To date, **FD-SOI** remains a niche market and is still trying to gain widespread adoption. But recently we observed significant moves in the arena, suggesting there is a place for **FD-SOI** in the market. Earlier this year, **Samsung** and **STMicroelectronics** signed a strategic agreement to expand 28nm **FD-SOI** technology. **GlobalFoundries**, a foundry for 28nm **FD-SOI**, plans to field a 14nm **FD-SOI** process after 2015. At the recent IEEE S3S Conference, **IBM** described an **SOI FinFET** technology at 10nm, which is said to be a more simple process than Bulk FinFET. On the Bulk FinFET front, **Intel** is shipping its 14nm FinFET technology, but with six months late due to yield issues. Other foundries are currently struggling with similar issues for their Bulk FinFETs at 16nm/14nm, and the challenges are expected to increase at 10nm and beyond. Therefore, it might be time to take a look at **IP situation of FD-SOI arena**, especially for the next stage of planar and FinFET devices.

This patent landscape focuses on fully depleted devices on SOI substrate for planar and FinFET architectures. More than **740 patent families** related to this field have been published worldwide up to October 2014. In the early 1990s, **IBM** filed first patents related to fully depleted transistors on SOI substrate. Those fundamental patents were followed by an ever increasing number of patent applications between 2000 and 2005 as more companies competed in FDSOI. After a 2005-2010 decrease period of patenting activity suggesting less room for breakthrough innovation, the patent applications are increasing again since 2010. This **second peak of patent publications** could be an indication of a **future ramp-up** of the FDSOI market.

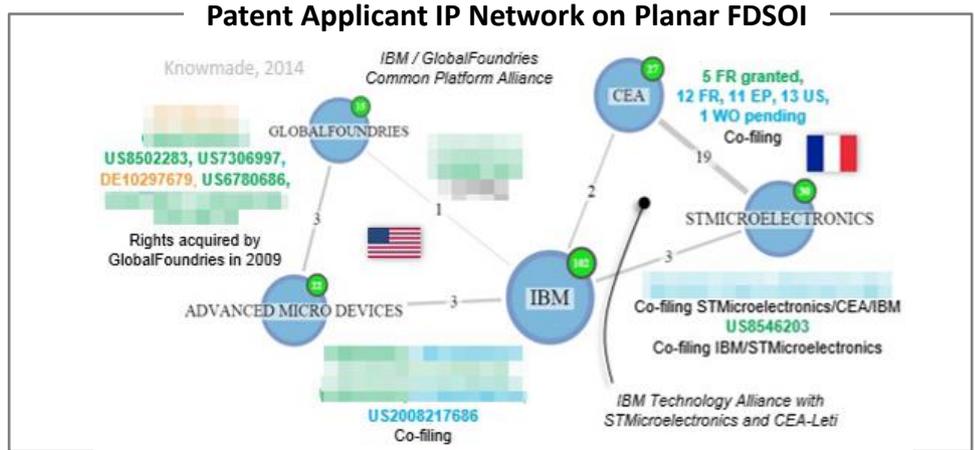


**Planar FDSOI** patented technologies account for more than **340 patent families** and they are monopolized by Americans (IBM, AMD, GlobalFoundries) and Europeans (STMicroelectronics, CEA-Leti). On the **SOI FinFET** (400+ patent families), we find IP players already involved in bulk FinFET technology (TSMC, Infineon, Samsung, Toshiba ...). The patent applicants are mainly **big players** already involved in microelectronic arena and there is very little room left for new IP comers. There are very few SME or startups, and the few number of academics involved in FDSOI patenting activities suggests a **mature technology**.

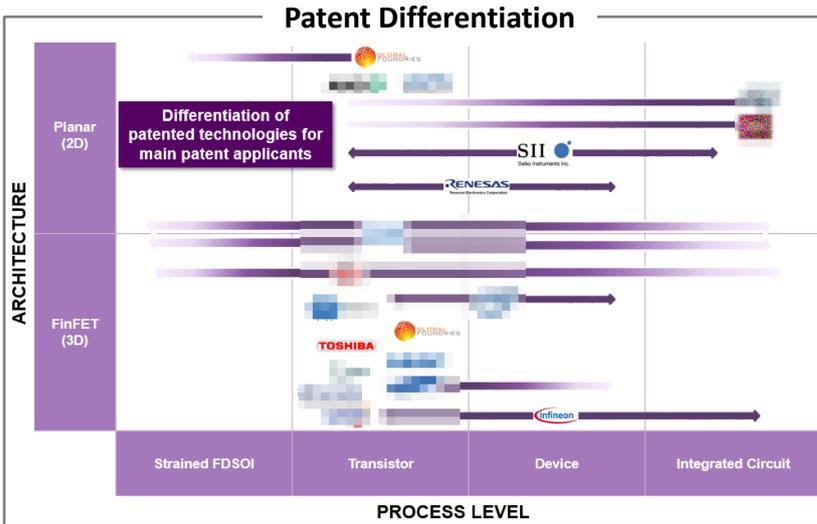
## IDENTIFY KEY PLAYERS AND COLLABORATIONS

More than 30 companies/academics are involved in FDSOI technology IP. **IBM**, a major proponent of the FDSOI, is **definitively leading** this patent landscape. **STMicroelectronics**, who played a pioneering role with its partners CEA-Leti and Soitec, has a **very young**, but promising, patent portfolio. **It is interesting** to find **FDSOI patents** held by **TSMC** and **Intel**, since they are rather known as proponents of the bulk-Si technology. This may suggest they have certainly carefully looked at FDSOI as a technology option, even if so far these companies do not support FDSOI. What could be their positions whether they want to enter the FDSOI market?

The report provides a **ranking** and analysis of the **relative strength** of the top FD-SOI technology patent holders derived from their portfolio size, patent citations networks, countries of patents filings, current legal status of patents and collaborations. Through thorough analysis we have identified five major players, each of which is profiled in this report. Each profile includes a detailed portfolio summary including market news, collaborations, product, roadmap, patenting activity, patented technologies with detailed recent innovations, key patents, and partnerships.



## PATENTED TECHNOLOGY AND IP STRATEGY



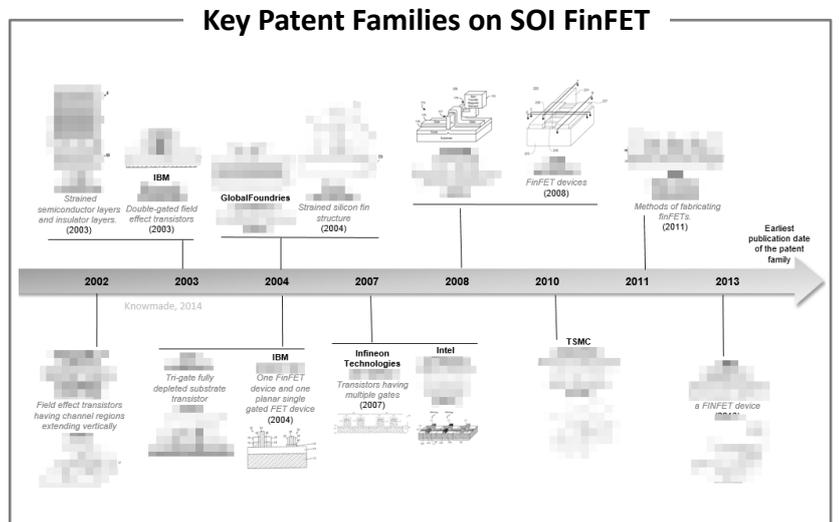
The 740+ patent families selected for this study have been **manually segmented** by architecture type (Planar FDSOI, SOI FinFET), and the dataset is organized into various technology segments that are analyzed (strained FD-SOI, transistor, device, integrated circuit). Methods for manufacturing transistor on SOI substrate represent the biggest part of patents, while recent patents seem to focus on IC level.

We observe a high number of **license agreements** and **collaborations** in FDSOI technology (IBM/ST, Samsung/ST, ST/CEA/Soitec, GF/ST ...), and for the moment there is **no patent litigation**, since the proponents of the FDSOI technology still attempt to gain its widespread adoption at 28-14nm nodes. But this could change when the FD-SOI technology will need to use FinFET-based approaches (SOI FinFET) at the 10nm node and beyond, since TSMC and Intel could enter in IP battle.

## IDENTIFY KEY PATENTS

More than **50 key patents** have been identified based on several indicators, including family size, legal status, citations analysis and impact on FD-SOI technology. **Key Patents** are mainly held by **IBM** whether on Planar FDSOI or SOI FinFET. In the future, **IBM** is expected to maintain its **leadership position** in the FDSOI patent landscape, while **STMicroelectronics** and **CEA-Leti** could **become major forces** in Planar FDSOI IP. **TSMC** and **Intel** also hold some key patents that they could assert at the right time.

Our report also includes an **Excel database** containing all of the analyzed patents. This database allows for multi-criteria searches and includes patent publication number, hyperlinks to the original documents, priority date, title, abstract, patent assignees, technological segments and legal status for each member of the patent family.



**COMPANIES CITED IN THE REPORT (NON-EXHAUSTIVE)**

Advanced Micro Devices, CEA-Leti, GlobalFoundries, IBM, IMEC, Infineon Technologies, Institute of Microelectronics (CAS), Intel, KAIST, Lapis Semiconductor, Micron Technology, Oki Electric Industry, Renesas Electronics, Samsung Electronics, Seiko Instruments, Sharp, SK Hynix, SMIC, Soitec, STMicroelectronics, Toshiba, TSMC, United Microelectronics Corporation...

**TABLE OF CONTENT****Scope Of the Report****Rational for Choice****Key Features of the Report****Terminology for Patent Analysis****Methodology****Patent Search Strategy****Technological Segmentation**

Architecture: planar FD-SOI AND SOI FinFET

Process level: transistor, device and circuit

**Executive Summary** p.16**I. FD-SOI Technology Overview** p.32**II. Patent Landscape** p.38

For each architecture (planar FD-SOI and SOI FinFET):

- Time Evolution of Patent Publications
- Countries of Patent Filings
- Time Evolution by Country of Patent Filing
- Main Patent Assignees Ranking
- Main Joint Developments and Collaborations
- Time Evolution of Patent Assignees
- Countries of Patent Filings for Main Patent Assignees
- Countries of Current Main Patent Holders
- Patent Assignee IP Network
- Summary of Main Assignee Patent Portfolio
- Strength of Main Assignee Patent Portfolio

- Leadership of Patent Applicants
- IP Blocking Potential of Applicants
- Potential Future Plaintiffs
- Key Patents
- Granted Patents Near Expiration
- Matrix Patent Assignees/Technology Segment
- Patent Differentiation

**III. Focus on Key Players** p.79

For all of key player: last news, main collaborations and joint developments, technology choices, portfolio summary, strength/weakness, key patents.

<b>IBM</b>	<b>p.80</b>
<b>STMicroelectronics/CEA/Soitec</b>	<b>P.87</b>
<b>Samsung</b>	<b>p.91</b>
<b>GlobalFoundries/Advanced Micro Devices (AMD)</b>	<b>p.94</b>
<b>TSMC</b>	<b>p.99</b>
<b>Intel</b>	<b>p.106</b>
<b>Micron Technology</b>	<b>p.111</b>
<b>Infineon Technologies</b>	<b>p.113</b>
<b>Renesas Electronics</b>	<b>p.116</b>
<b>Seiko Instruments</b>	<b>p.119</b>
<b>Lapis Semiconductor/Oki Semiconductor</b>	<b>p.120</b>

**Conclusions** p.121**Annexes** p.123**AUTHORS**

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## FD-SOI Patent Landscape

*Fully Depleted Transistors on SOI Substrate*

December 2014

### SHIP TO

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Job Title:

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City:

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Country:

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2.2 Some weeks prior to the release date the Seller can propose a pre-release discount to the Buyer.

The Seller shall by no means be responsible for any delay in respect of article 2.2 above, and including in cases where a new event or access to new contradictory information would require for the analyst extra time to compute or compare the data in order to enable the Seller to deliver a high quality Products.

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2.4 The mailing is operated through electronic means either by email via the sales department. If the Product’s electronic delivery format is defective, the Seller undertakes to replace it at no charge to the Buyer provided that it is informed of the defective formatting within 90 days from the date of the original download or receipt of the Product.

2.5 The person receiving the Products on behalf of the Buyer shall immediately verify the quality of the Products and their conformity to the order. Any claim for apparent defects or for non-conformity shall be sent in writing to the Seller within 8 days of receipt of the Products. For this purpose, the Buyer agrees to produce sufficient evidence of such defects.

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BIC or SWIFT code: CCBPFRPPNCE

IBAN: : FR76 1560 7000 6360 6214 5695 126

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4.2 The Seller shall only be liable for (i) direct and (ii) foreseeable pecuniary loss, caused by the Products or arising from a material breach of this agreement

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b) any claim attributable to errors, omissions or other inaccuracies in the Product or interpretations thereof.

4.4 All the information contained in the Products has been obtained from sources believed to be reliable. The Seller does not warrant the accuracy, completeness adequacy or reliability of such information, which cannot be guaranteed to be free from errors.

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